CS451/CS551/ECE441/ECE541 - Advanced Computer Architecture Course Syllabus Fall 2023

Instructor: Bob Rinker, Moscow - JEB 324, CdA - NIC Hedlund 202

rinker@uidaho.edu,(208) 885-7378
http://www2.cs.uidaho.edu/~rinker

Text: Computer Architecture - A Quantitative Approach, 6th Ed, by Hennessy and Patterson

Zoom ID: 830 1263 1661

Lec]	Day		Topic	Text/Ref
1	Aug	21	M	Introduction	
2	_	23	W	Quantitative Principles in Computer Design	Chap 1
3		25	F	Performance measurements, price/performance	Chap 1
4		28	M	Instruction Set Principles	Appendix A
5		30	W	Instruction Set Principles	Appendix A
6	Sep	1	F	Pipelining Concepts 1	Appendix C
		4	M	**** Labor Day - NO Classes ****	
7		6	W	Pipelining Concepts	Appendix C
8		8	F	Pipelining Concepts - performance concepts	Appendix C
9		11	M	Pipelining Concepts - performance concepts	Appendix C
10		13	W	Instruction-Level parallelism - concepts	Chap 3
11		15	F	Exploiting Instruction-Level parallelism	Chap 3
12		18	M	ILP - Dynamic scheduling	Chap 3
13		20	W	ILP - Dynamic scheduling	Chap 3
14		22	F	ILP - Dynamic scheduling	Chap 3
15		25	M	Exploiting ILP with software	Chap 3
16		27	W	Exploiting ILP with software	Chap 3
17		29	F	Memory hierarchy - caches	Appendix B
18	Oct	2	M	Memory hierarchy - caches	Appendix B
19		4	W	Memory hierarchy - optimizing performance	Chap 2
		6	F	**** Test 1 ****	
20		9	M	Virtual Memory	Chap 2
21		11	W	Virtual Memory	Chap 2
		13	F	**** Exam Review ****	
22		16	M	Memory performance optimization	Chap 2
23		18	W	Memory performance optimization	Chap 2
24		20	F	Memory performance optimization	Chap 2
25		23	M	Data-Level Parallelism	Chap 4
26		25	W	Data-Level Parallelism	Chap 4
27		27	F	Data-Level Parallelism	Chap 4
28		30	M	Multiprocesors	Chap 5
29	Nov	1	W	Multiprocesors - thread-level parallelism	Chap 5
30		3	F	Multiprocesors - thread-level parallelism	Chap 5
31		6	M	Multiprocesors - thread-level parallelism	Chap 5
32		8	W	Multiprocesors - thread-level parallelism	Chap 5
33		10	F	Multiprocesors - thread-level parallelism	Chap 5
		13	M	**** Test 2 ****	
34		15	W	Storage Systems	Appendix D
35		17	F	Storage Systems	Appendix D
	Nov	20 -	- 24	****Thanksgiving Break - NO Classes****	
		27	M	**** Exam Review ****	
36	-	29	W	Storage Systems	Appendix D
37	Dec	1	F	Storage Systems	Appendix D
38		4	M	Embedded Systems	Appendix E
39		6	W	Embedded Systems	Appendix E
40		8	F	Course Summary - Final Exam Review	

Final Exam: Thursday, December 14, 12:45 - 2:45 pm

Grading:

	CS551/ECE541	CS451/ECE441
Two Midterm Tests	40%	50%*
Final Exam	20%	25%
Assignments	20%	25%
Term Project	20%	*
Total	100%	100%

The letter grade you receive from the course will be determined as follows:

90%	-	100%	A
89.9%	-	80%	В
79.9%	-	70%	C
69.9%	-	60%	D
59.9%	-	0%	F

The instructor reserves the right to adjust these percentages lower if deemed necessary.

Center for Disability Access and Resources Reasonable Accommodations Statement:

University of Idaho is committed to ensuring an accessible learning environment where course or instructional content are usable by all students and faculty. If you believe that you require disability-related academic adjustments for this class (including pregnancy-related disabilities), please contact Center for Disability Access and Resources (CDAR) to discuss eligibility. A current accommodation letter from CDAR is required before any modifications, above and beyond what is otherwise available for all other students in this class will be provided. Please be advised that disability-related academic adjustments are not retroactive. CDAR is located at the Bruce Pitman Building, Suite 127. Phone is 208-885-6307 and e-mail is cdar@uidaho.edu. For a complete listing of services and current business hours visit https://www.uidaho.edu/cdar

- Pitman 127
- 208-885-6307
- website at <www.uidaho.edu/cdar>

^{* -} CS451/ECE441 students may substitute a project in lieu of one of the midterm tests.