CS451/CS551/ECE441/ECE541 - Advanced Computer Architecture

Course Syllabus Fall 2015

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Text: *Computer Architecture - A Quantitative Approach*, 5th Ed, by Hennessy and Patterson

Lec	Day			Topic	Text/Ref
1	Aug	24	M	Introduction	
2		26	W	Quantitative Principles in Computer Design	Chap 1
3		28	F	Performance measurements, price/performance	Chap 1
4		31	M	Instruction Set Principles	Appendix A
5	Sep	2	W	Instruction Set Principles	Appendix A
6		4	F	Pipelining Concepts	Appendix C
	Sep	7	M	**** Labor Day - NO Classes ****	
7		9	W	Pipelining Concepts	Appendix C
8		11	F	Pipelining Concepts - performance concepts	Appendix C
9		14	M	Pipelining Concepts - performance concepts	Appendix C
10		16	W	Instruction-Level parallelism - concepts	Chap 3
11		18	F	Exploiting Instruction-Level parallelism	Chap 3
12		21	M	ILP - Dynamic scheduling	Chap 3
13		23	W	ILP - Dynamic scheduling	Chap 3
14		25	F	ILP - Dynamic scheduling	Chap 3
15		28	M	Exploiting ILP with software	Chap 3
16		30	W	Exploiting ILP with software	Chap 3
17	Oct	2	F	Memory hierarchy - caches	Appendix B
18		5	M	Memory hierarchy - caches	Appendix B
19		7	W	Memory hierarchy - optimizing performance	Chap 2
		9	F	**** Test 1 ****	
20		12	M	Virtual Memory	Chap 2
21		14	W	Virtual Memory	Chap 2
		16	F	**** Exam Review ****	
22		19	M	Memory performance optimization	Chap 2
23		21	W	Memory performance optimization	Chap 2
24		23	F	Memory performance optimization	Chap 2
25		26	M	Data-Level Parallelism	Chap 4
26		28	W	Data-Level Parallelism	Chap 4
27		30	F	Data-Level Parallelism	Chap 4
28	Nov	2	M	Multiprocesors	Chap 5
29		4	W	Multiprocesors - thread-level parallelism	Chap 5
30		6	F	Multiprocesors - thread-level parallelism	Chap 5
31		9	M	Multiprocesors - thread-level parallelism	Chap 5
32		11	W	Multiprocesors - thread-level parallelism	Chap 5
33		13	F	Multiprocesors - thread-level parallelism	Chap 5
		16	M	**** Test 2 ****	
34		18	W	Storage Systems	Appendix D
35		20	F	Storage Systems	Appendix D
	Nov	23 - 27		****Thanksgiving Break - NO Classes****	
		30	M	**** Exam Review ****	
36	Dec	2	W	Storage Systems	Appendix D
37		4	F	Storage Systems	Appendix D
38		7	M	Embedded Systems	Appendix E
39		9	W	Embedded Systems	Appendix E
40		11	F	Course Summary - Final Exam Review	

Final Exam: Thursday, December 17, 12:30-2:30 pm

Grading:

	CS551/ECE541	CS451/ECE441
Two Midterm Tests	40%	50%*
Final Exam	20%	25%
Assignments	20%	25%
Term Project	20%	*
Total	100%	100%

The letter grade you receive from the course will be determined as follows:

90%	-	100%	A
89.9%	-	80%	B
79.9%	-	70%	C
69.9%	-	60%	D
59.9%	-	0%	F

The instructor reserves the right to adjust these percentages lower is deemed necessary.

* - CS451/ECE441 students may substitute a project in lieu of one of the midterm tests.

Disability Support Services Reasonable Accommodations Statement:

Reasonable accommodations are available for students who have documented temporary or permanent disabilities. All accommodations must be approved through Disability Support Services located in the Idaho Commons Building, Room 306 in order to notify your instructor(s) as soon as possible regarding accommodation(s) needed for the course.

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