

CS451/EE441/CS551/EE541 - Advanced Computer Architecture

Course Syllabus

Fall 2008

Instructor: Bob Rinker, JEB B28, rinker@cs.uidaho.edu

Class Web Site: www.cs.uidaho.edu/~rinker/cs551

Text: *Computer Architecture - A Quantitative Approach*, 4th Ed, by Hennessey and Patterson

Lec	Topic	Text/Ref
1	Introduction	
2	Instruction Set Principles	App J
3	Pipelining Concepts	App A
4	Pipelining Concepts - performance concepts	App A
5	Pipelining Concepts - performance concepts	App A
6	Pipelining Concepts - performance concepts	App A
7	Instruction-Level parallelism - concepts	Chap 2
8	Exploiting Instruction-Level parallelism	Chap 2
9	ILP - Dynamic scheduling	Chap 2
10	Limits on ILP	Chap 3
11	Limits on ILP	Chap 3
12	Limits on ILP	Chap 3
13	Exploiting ILP with software **** Test 1 ****	App G
14	Multiprocessors	Chap 4
15	Multiprocessors - thread-level parallelism	Chap 4
16	Multiprocessors - thread-level parallelism	Chap 4
17	Multiprocessors - thread-level parallelism	Chap 4
18	Memory hierarchy - caches	App C
19	Virtual Memory	App C
20	Virtual Memory	App C
21	Memory performance optimization	Chap 5
22	Memory performance optimization	Chap 5
23	Memory performance optimization	Chap 5
24	Storage Systems **** Test 2 ****	Chap 6
25	Storage Systems	Chap 6
26	Storage Systems	Chap 6
27	Interconnection Networks and Clusters	App E
28	Interconnection Networks and Clusters	App E

Grading:

	CS551/EE541	CS451/EE441
Two Hour Tests	40%	50%
Final Exam	20%	25%
Assignments	15%	25%
Term Project	25%	
Total	100%	100%

The letter grade you receive from the course will be determined as follows:

90%	-	100%	A
89.9%	-	80%	B
79.9%	-	70%	C
69.9%	-	60%	D
59.9%	-	0%	F

The instructor reserves the right to adjust these percentages lower is deemed necessary.