• Project/Programming Oriented Projects
  – Develop a pipelined RISC Simulator
  – Develop a pipelined and bypassed Simulator
  – Simulate cache performance for a set of codes
  – Simulate/compare various cache coherence protocols
  – Develop a superscalar RISC simulator using Tomasulo’s algorithm
  – Develop a superscalar RISC simulator using Scoreboarding
  – Develop a superscalar RISC simulator using simultaneous multithreading

• Research Oriented Projects - Possible topics
  – Chip Multiprocessors
  – Simultaneous multithreading
  – Branch prediction using trace caches
  – VLIW Architectures
  – Things to do with a billion transistors
  – DSP Architectures
  – Survey of cache configurations
  – Dataflow architectures
  – Fine-grained execution architectures
  – Cache coherency in multiprocessors
  – Dynamic compilation (Transmeta)
  – Multimedia Instruction Sets
  – Reconfigurable Computing
  – Formal methods verification of computer architectures
  – GPU Architectures
  – "Game Box" architectures
  – Hypertransport(AMD)/QPI(Intel) interconnect buses