CS451/551/ECE441/541 - Advanced Computer Architecture
Assignment #6 - Fall 2023

1. Consider the following C code:

```
double A[16], B[16], C[16];
double X, Y;
int i;
   .
   .

for(i = 0; i < 16; i++)
   C[i] = X * A[i] + Y * B[i];
```

a) Write a RISC-V assembly program that implements this loop, using the standard (non-vector) instruction set. Count the number of floating point instructions that will be executed in performing this loop.

b) Write a version of this loop using a RISC-V model that has vector instructions. Use the vector op-codes listed in Figure 4.2 . Count the number of floating point instructions that will be executed in performing this code.

2. In the cache coherence protocol that the book describes (e.g., in Figure 5.6), it assumes that a write hit and a write miss are treated the same. A popular protocol called MESI adds an additional state (**M**odified) to the protocol. What advantage does this protocol have compared to the one in the book? Draw the resulting state machine diagram (similar to Figure 5.6).