CS451/551/ECE441/541 - Advanced Computer Architecture Assignment #4 - Fall 2019

1. For the following questions, use the following string of address references given as *word* adddress:

1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17

- Assuming a direct mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or miss, and show the final contents of the cache.
- Assuming a direct mapped cache with 4-word blocks and a *total size* of 16 words, show the hits and misses and final cache contents.
- Assuming a two-way set associative cache with one-word blocks and a *total size* of 16 words, show the hits and misses and final cache contents. Assume LRU replacement.
- Assuming a fully associative cache with one-word blocks and a total size of 16 words, show the hits and misses and final cache contents.
- 2. You purchased an Acme computer with the following features:
 - 95% of all memory accesses are found in the cache.
 - Each cache block is two words, and the entire block is read on any miss.
 - The processor sends references to its cache at the rate of 10^9 words per second.
 - 25% of those references are writes.
 - Assume that the memory system can support 10^9 words per second, reads or writes.
 - The bus reads or writes a single word at a time (the memory system cannot read or write two words at once.
 - Assume at any one time, 30% of the blocks in the cache are dirty.
 - The cache uses write allocate on the write miss.

3. You are considering adding a peripheral to the system and you want to know how much of the memory bandwidth is already used. Calculate the percentage of memory system bandwidth used on the average, for:

- The cache is write through.
- The cache is write back.

State any assumptions you make in developing your answer.