

UI CS451/551/ECE441/541/WSU CptS 561/EE524
Advanced Computer Architecture

Assignment #4

1. In the cache coherence protocol that the book describes (e.g., in Figure 4.6 on page 214), it assumes that a write hit and a write miss are treated the same. It also alludes to the possibility where they are treated separately. Such a protocol adds an additional state (**M**odified) to the protocol, and is called *MESI*, for the four possible states. Draw the state diagram for this protocol. What advantage does this protocol have over the one in Figure 4.6?

2. Assume a directory-based cache coherence protocol. The directory currently has information that indicates the processor P1 has the data in “exclusive” mode. If the directory now gets a request for the same cache block from processor P1, what could this mean? What should the directory controller do?. Such cases are called “race conditions” and are the reason why coherence protocols are so hard to design and verify.)

3. As discussed in class, the directory controller can send invalidates for lines that have been replaced by the local cache controller. To avoid such messages and to keep the directory consistent, replacement hints are used. Such messages tell the controller that a block has been replaced. Modify the directory coherence protocol to use such replacement hints.