CS451/551/ECE441/541   Advanced Computer Architecture

Assignment #2
Fall 2023

1. Suppose we are considering a change to an instruction set. The base machine initially has only loads and stores to memory, and all operations work on the registers. Measurements of the load-store machine showing the *instruction mix* and clock cycle counts per instruction are given in the table below:

Instruction Type	Frequency	Clock Cycle Count
ALU Operations	43%	1
Loads	21%	2
Stores	12%	2
Branches	24%	2

Assume that 25% of the *ALU Operations* directly use a loaded operand that is not used again.

We propose adding ALU instructions that have one source operand in memory. These new *register-memory instructions* have a clock cycle count of 2. Suppose that the extended instruction set increases the clock cycle count for branches by 1 (so branches now take 3 cycles total), but it does not affect the clock cycle time. Would this change improve CPU performance? Justify your answer by showing your work.

2. Consider the following code fragment:

```
loop: ld   x1, 0(x2)
      addi x1, x1, #1
      sd   0(x2), x1
      addi x2, x2, #4
      sub  x4, x3, x2
      bne  x4, x0, loop
```

a) Show the timing (total number of clock cycles to execute) of executing this sequence on a four/five stage (non-pipelined) RISC-V processor. Note that some instructions will only require four of the possible five stages.

b) Show the timing of this instruction sequence for a processor that uses the 5-stage RISC-V pipeline, but without any data forwarding and without a delayed branch slot. Determine the number of cycles required to execute this loop. For pipelined processors, a count of the number of clock cycles is usually taken from the first cycle of the first instruction, to the first cycle of the last instruction, even though the last instruction will require a few more cycle to complete.

c) Show the timing of this instruction sequence with all possible forwarding and bypassing hardware, and with a single-cycle delayed branch slot. Determine the number of cycles required to execute this loop.

d) Calculate the Speedups of the pipelined machines vs the original one.