For this exercise, you will be building a 16 bit ALU, using a modification of the single-bit ALU you built for the last assignment. This ALU should perform the same functions on 16-bit numbers as your single-bit ALU did on 1-bit values. The ADD and SUB functions should perform 2's complement operations. You should assume the same gate delays as before in modelling your design.

In order to reduce propagation delay, your 16-bit ALU should use a 4-bit carry look-ahead circuit, rather than the ripple adder that would result from simply instantiating your 1-bit ALU.

As before, you should turn in your design in a single vhdl source file. As part of this assignment, determine the difference in the propagation delay that results from using the carry-lookahead as compared with the ripple adder, and report on this difference in the comments in your VHDL file.