Using VHDL, you are to design an expandable, 1-bit ALU, similar to the one we discussed in class. It should accept two 1-bit inputs, A and B, and perform the following functions:

A AND B
A OR B
A
B
NOT B
A + B
A − B

Your ALU should be considered as a “bit slice”, which can be replicated and connected to produce a multiple-bit ALU. The signals necessary to do this should be included in your design.

Your design should be structural in nature. Assume that the gate delay is 2 ns.