Chapter 1 - Hardware Concepts

Stallings, 9e

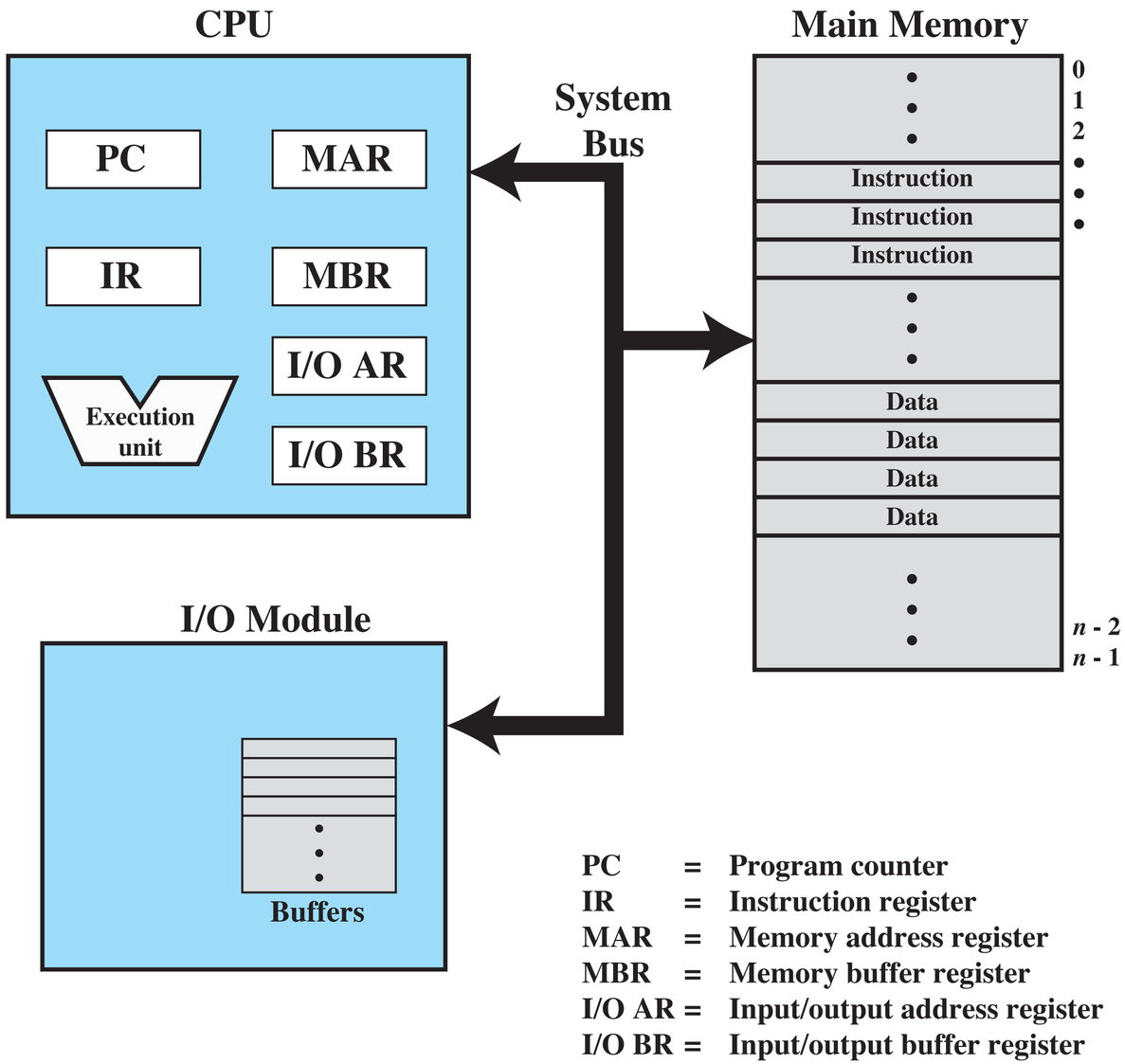


Figure 1.1 Computer Components: Top-Level View

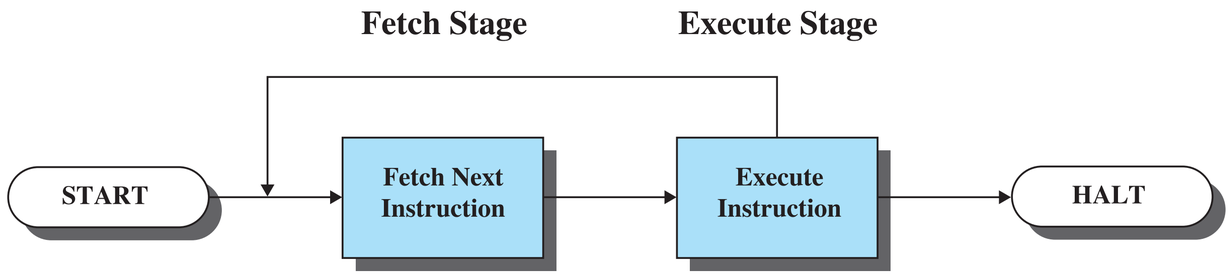


Figure 1.2 Basic Instruction Cycle

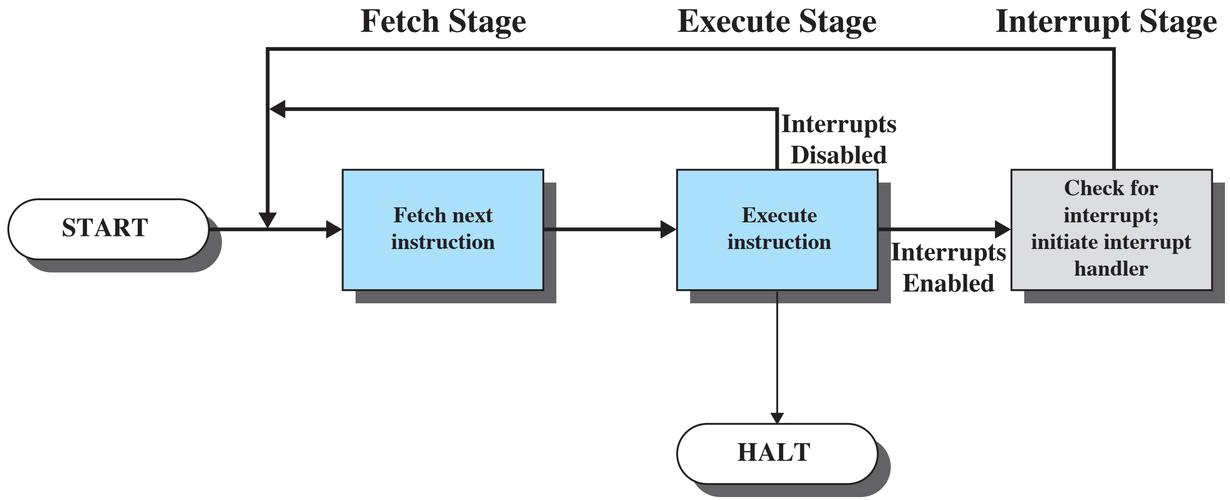


Figure 1.7 Instruction Cycle with Interrupts

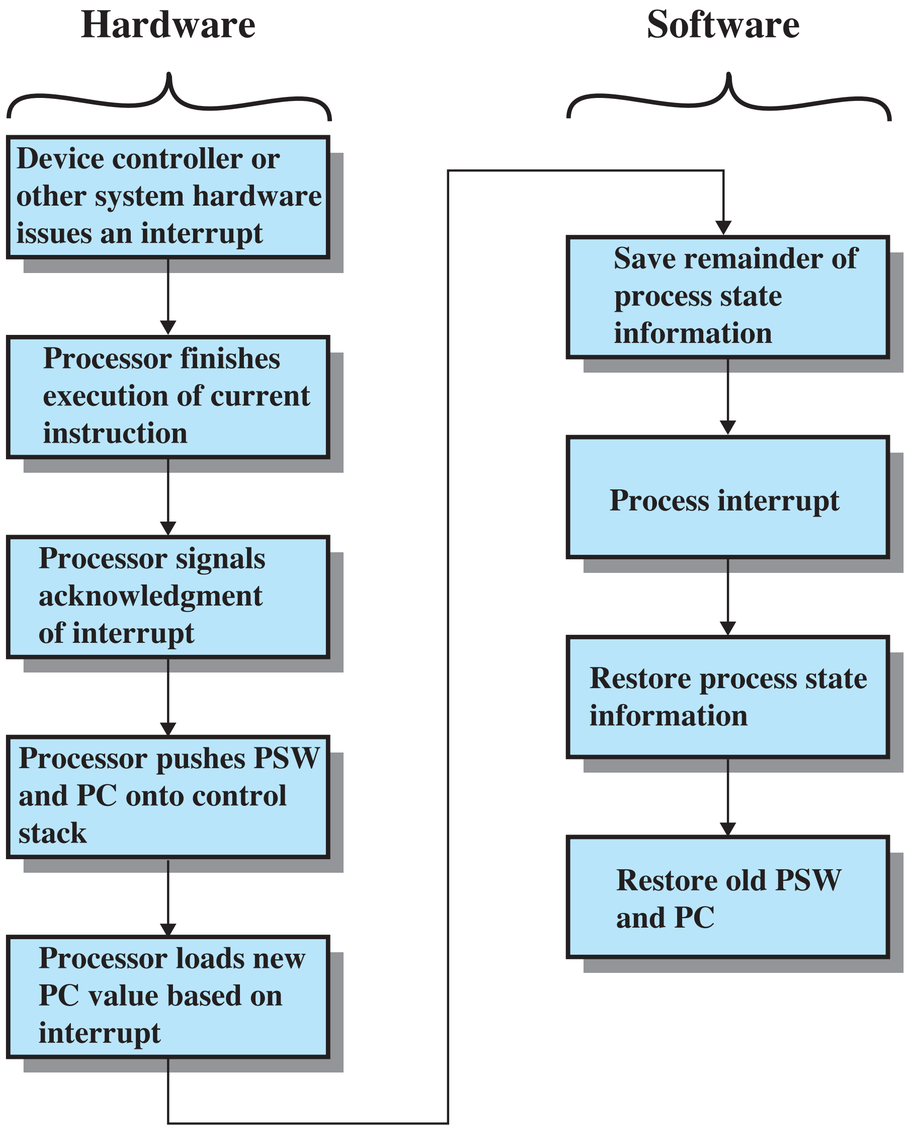


Figure 1.10 Simple Interrupt Processing

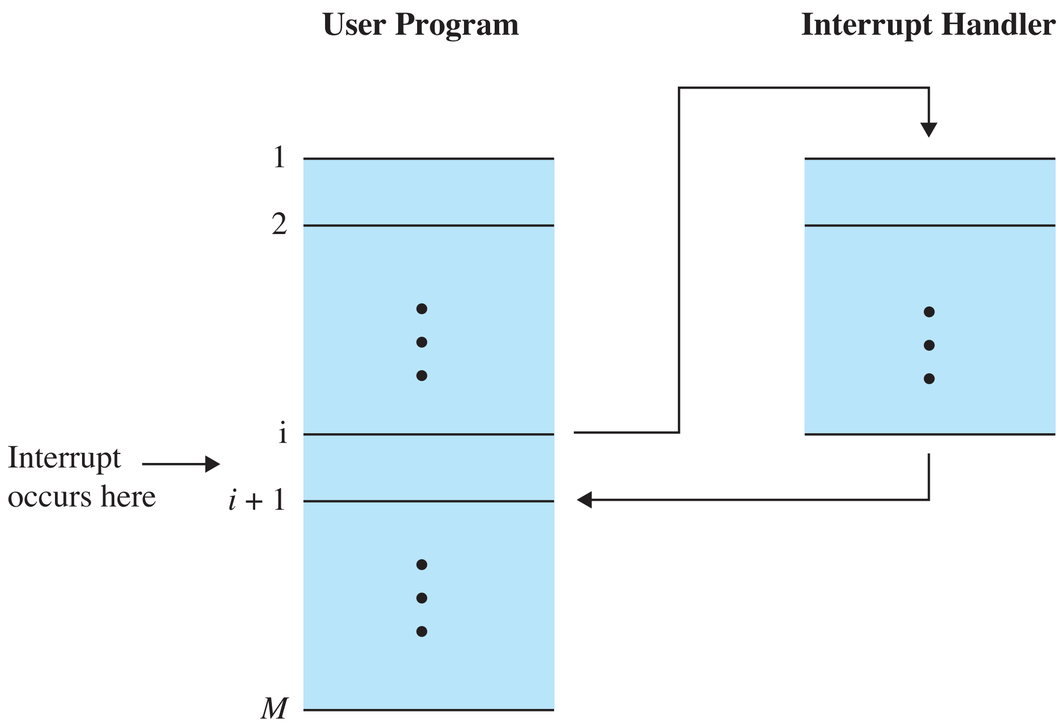
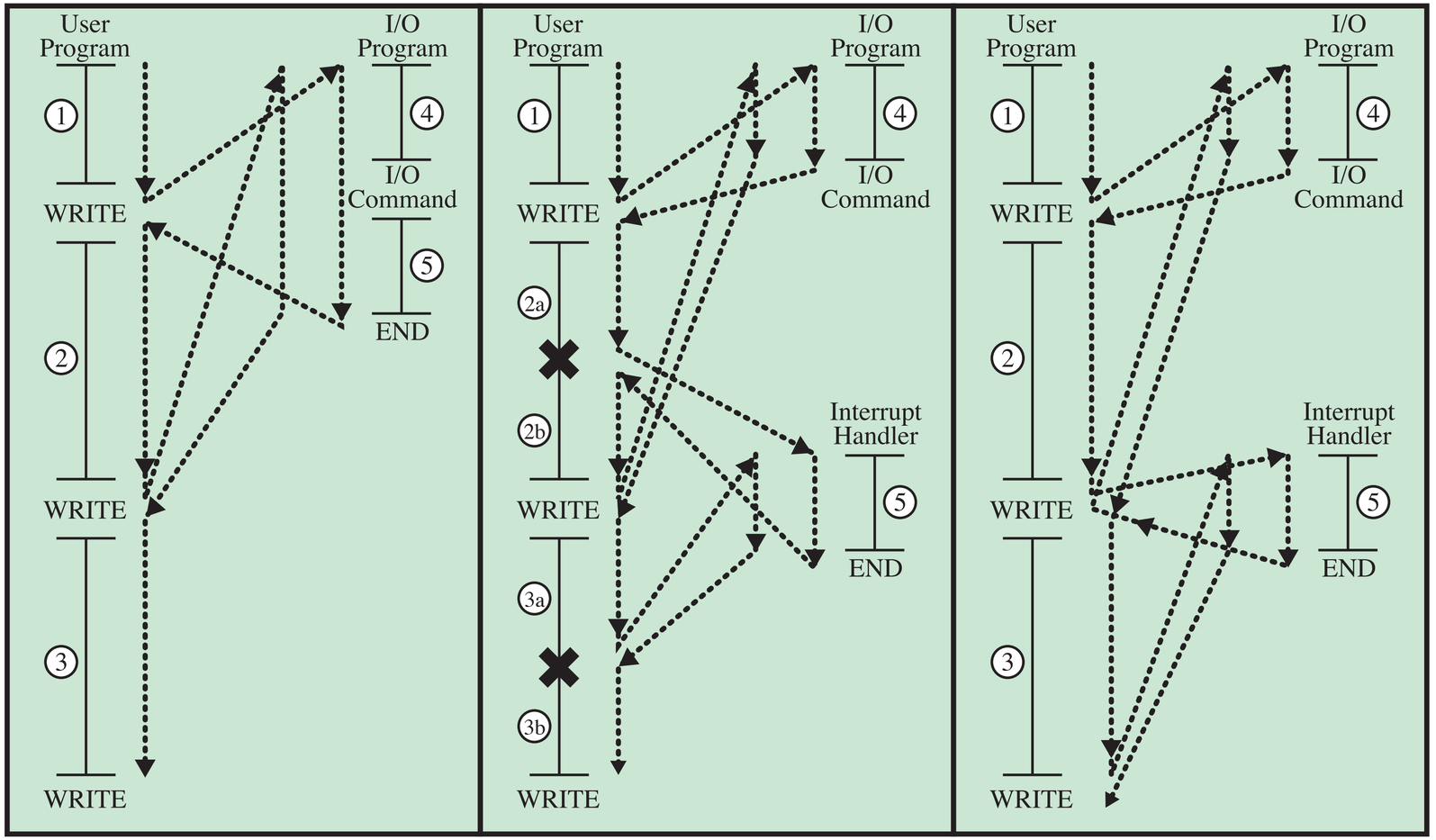


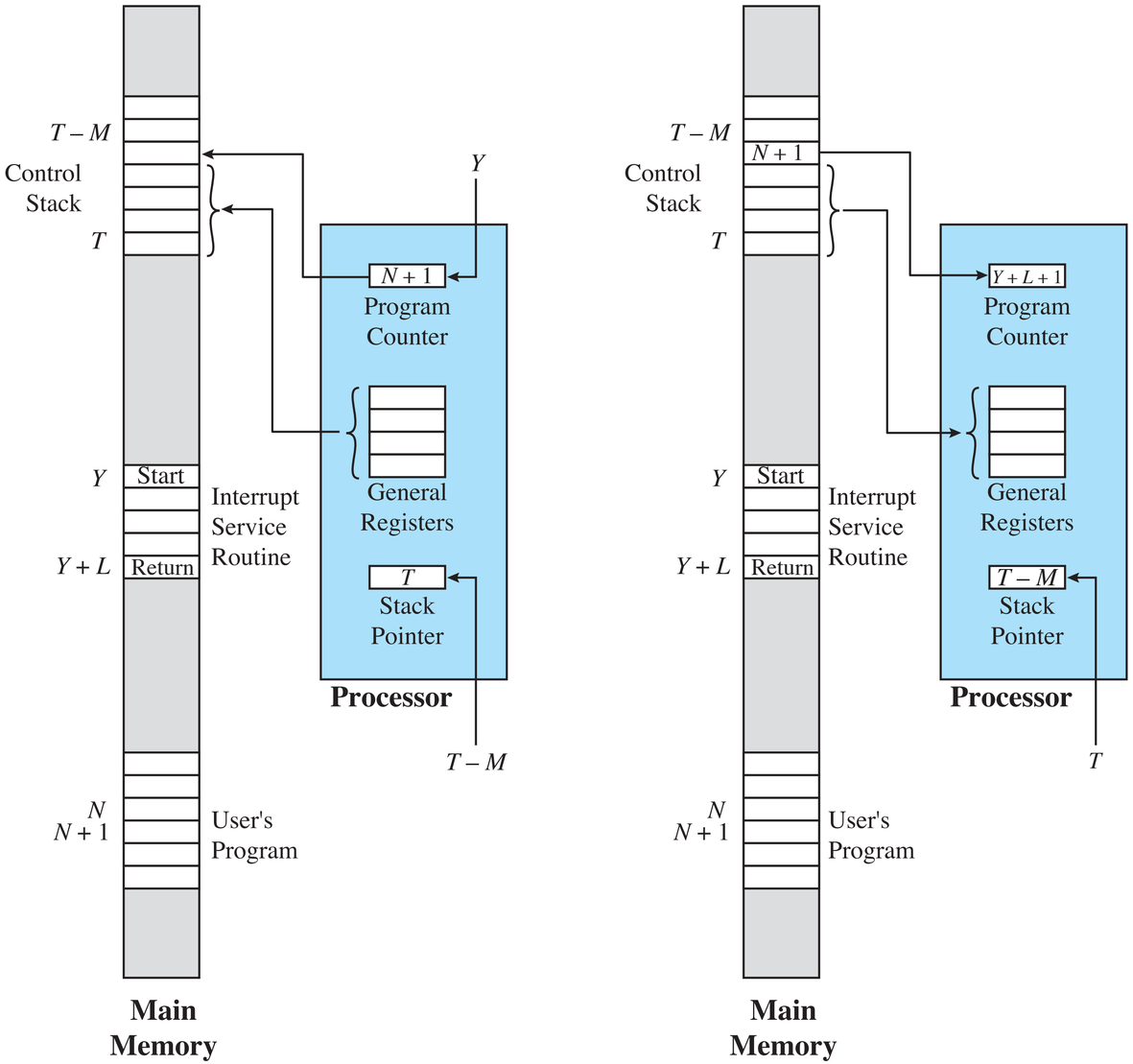
Figure 1.6 Transfer of Control via Interrupts



(a) No interrupts (b) Interrupts; short I/O wait (c) Interrupts; long I/O wait

✖ = interrupt occurs during course of execution of user program

Figure 1.5 Program Flow of Control Without and With Interrupts



(a) Interrupt occurs after instruction at location *N*

(b) Return from interrupt

Figure 1.11 Changes in Memory and Registers for an Interrupt

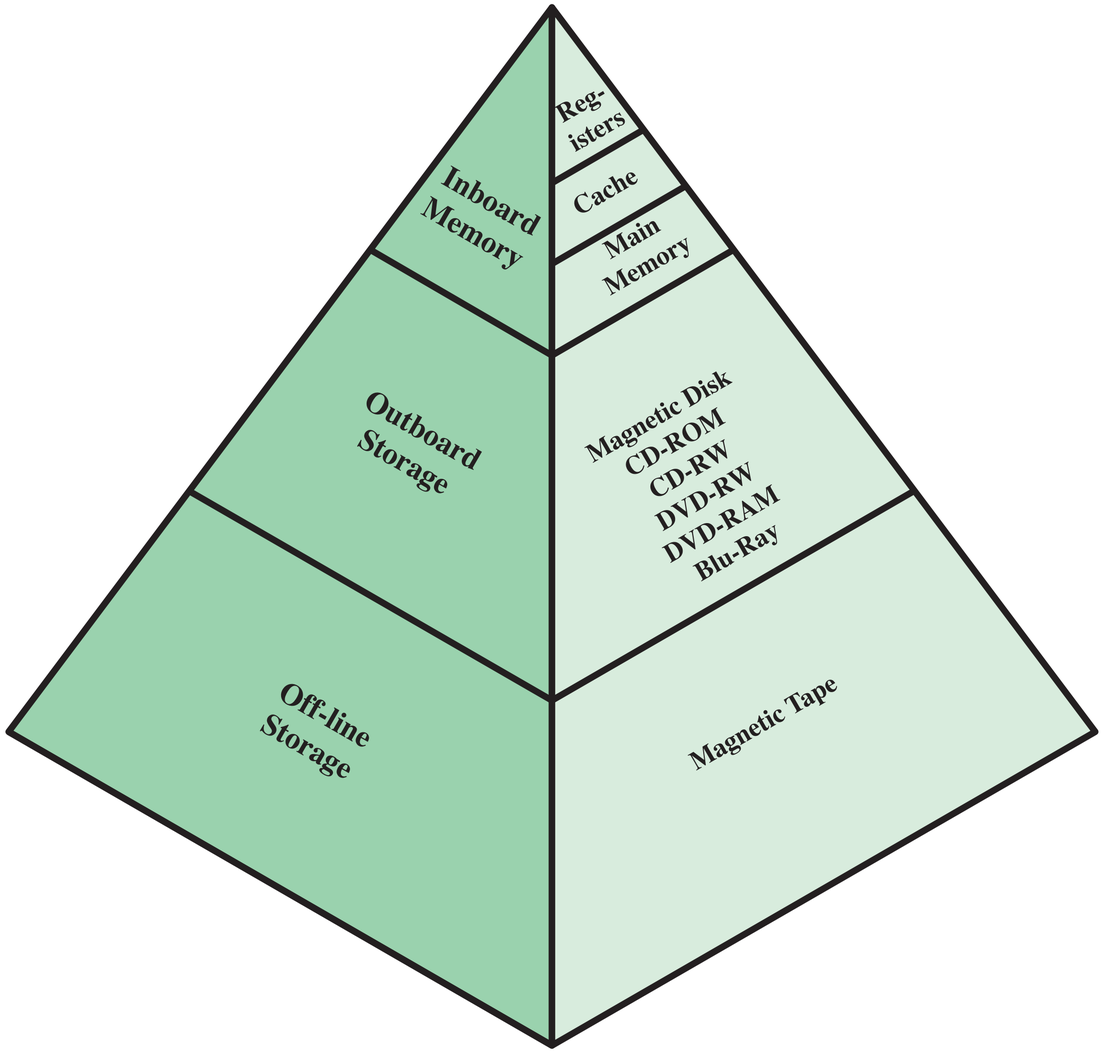
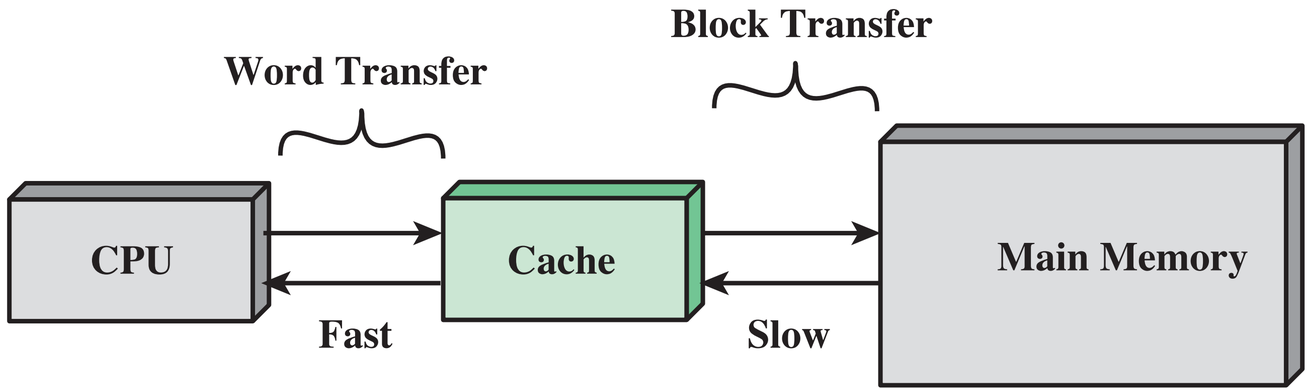
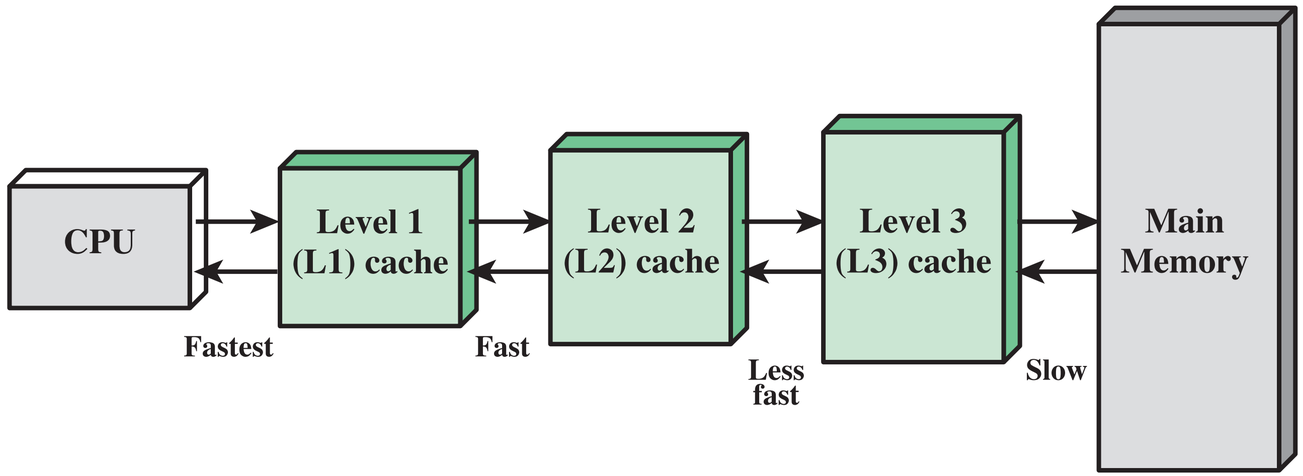


Figure 1.14 The Memory Hierarchy



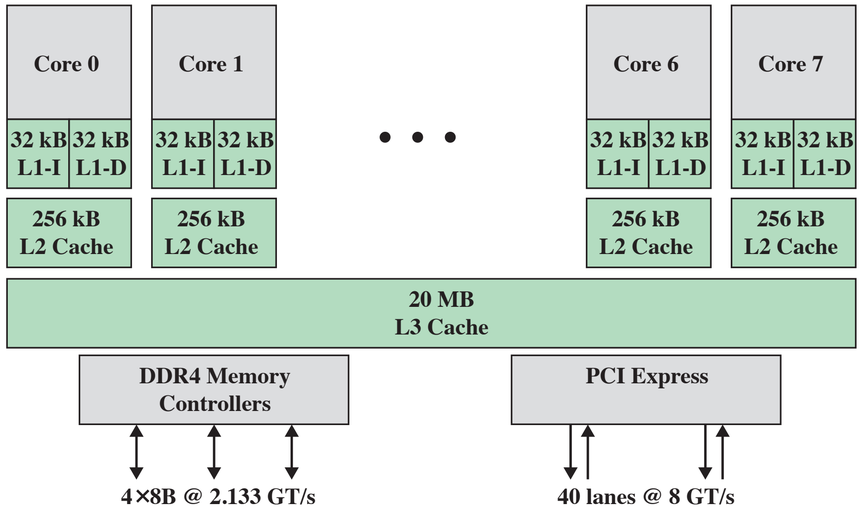
(a) Single cache



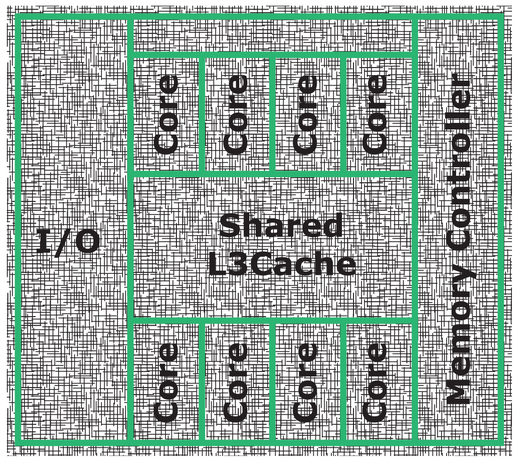
(b) Three-level cache organization

Figure 1.16 Cache and Main Memory

Multicore Processor



(a) Block diagram



(b) Physical layout on chip

Figure 1.20 Intel Core i7-5960X Block Diagram