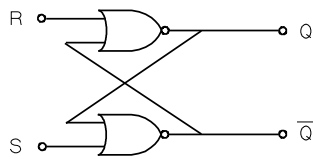
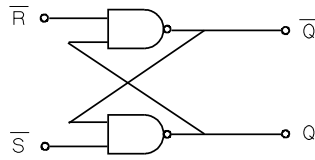


## A Couple of Interesting Circuits



R	S	Q	Q̄
0	0	Q	Q̄
0	1	1	0
1	0	0	1
1	1	0*	0*



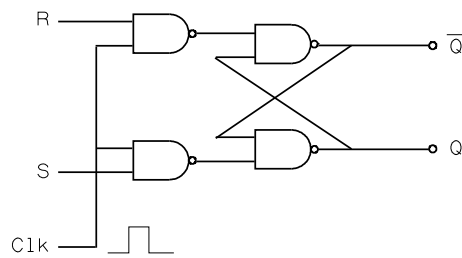
R̄	S̄	Q	Q̄
0	0	1*	1*
0	1	0	1
1	0	1	0
1	1	Q	Q̄

These circuits are called S-R (Set-Reset) Flip Flops

M3S20002

EE for EE

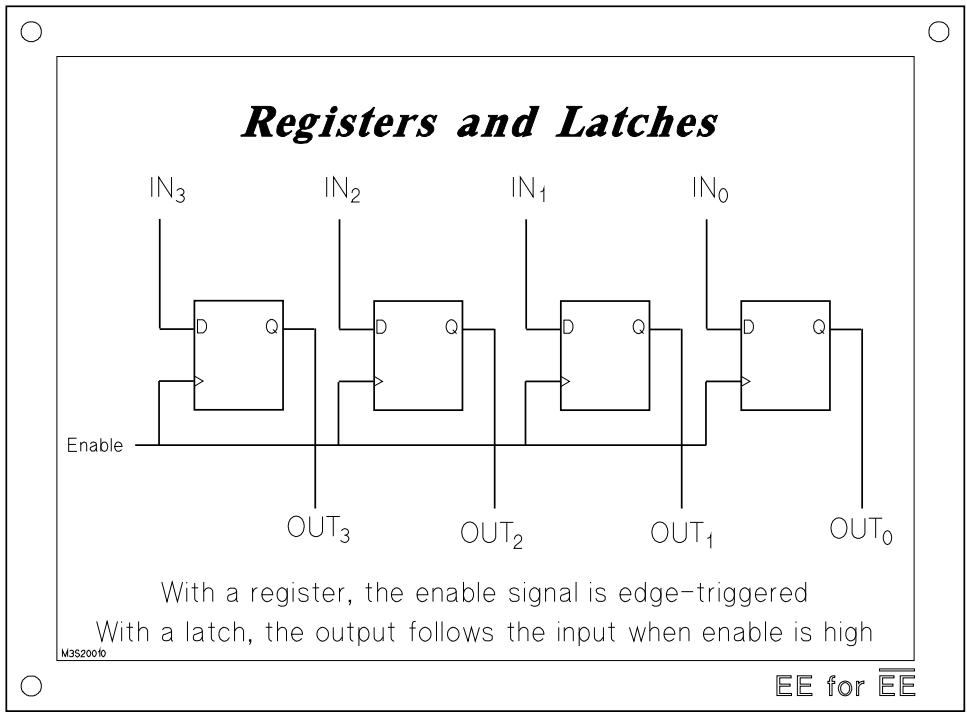
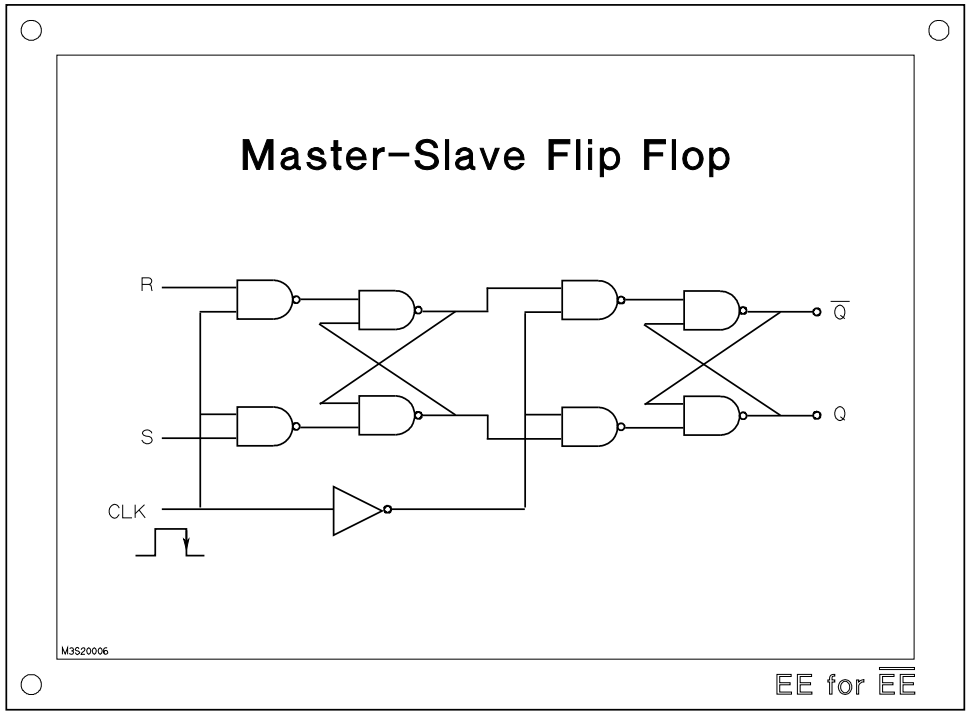
## Clocked S-R Flip Flop



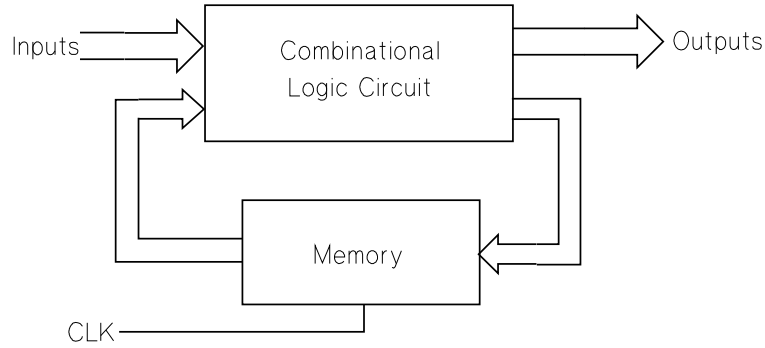
R and S inputs are "active" only when clock is high

M3S20003

EE for EE



## ***Synchronous Sequential Circuits***



*The current output depends on both the present inputs and current and previous outputs*

M3S2001f

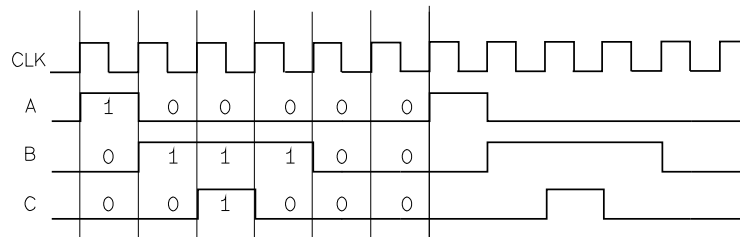
EE for EE

## ***An Example Sequential Circuit***

### *A Waveform Generator*

The problem:

Design a circuit which, given a clock signal, will produce the following repeating sequence of outputs



M3S2001e

EE for EE

## ***Sequential Circuit Design***

1. First, determine the number of states needed. One state is represented by one clock period. Our waveform repeats every six clock pulses, so we need six states. It will require 3 F/F's to represent six states.

2. Generate a state table showing current and next states:

s	s <sup>N</sup>
1	2
2	3
3	4
4	5
5	6
6	1

(NOTE: for this type of problem, this is a trivial step!)

M3S2003

EE for EE

## ***Sequential Circuit Design (Con't)***

3. Make a state assignment – that is, determine the binary combination of F/F outputs that will be used to represent each state. There is no unique state assignment. Then fill in the state table with proper current and next state values:

Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	s	s <sup>N</sup>	Q <sub>1</sub> <sup>N</sup>	Q <sub>2</sub> <sup>N</sup>	Q <sub>3</sub> <sup>N</sup>
0	0	0	1	2	0	0	1
0	0	1	2	3	0	1	0
0	1	0	3	4	0	1	1
0	1	1	4	5	1	0	0
1	0	0	5	6	1	0	1
1	0	1	6	1	0	0	0

M3S2004

EE for EE

## *Sequential Circuit Design (Con't)*

4. Develop the equations for each next-state variable:

$$Q_1^N = \overline{Q_1}Q_2Q_3 + Q_1\overline{Q_2}\overline{Q_3}$$

$$Q_2^N = \overline{Q_1}\overline{Q_2}Q_3 + \overline{Q_1}Q_2\overline{Q_3}$$

$$Q_3^N = \overline{Q_3}$$

5. ... and the circuit outputs:

$Q_1$	$Q_2$	$Q_3$	S	A	B	C
0	0	0	1	1	0	0
0	0	1	2	0	1	0
0	1	0	3	0	1	1
0	1	1	4	0	1	0
1	0	0	5	0	0	0
1	0	1	6	0	0	0

$$A = \overline{Q_1}\overline{Q_2}\overline{Q_3}$$

$$B = \overline{Q_1}\overline{Q_2}Q_3 + \overline{Q_1}Q_2\overline{Q_3} + \overline{Q_1}Q_2Q_3$$

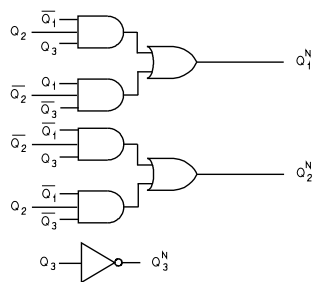
$$C = \overline{Q_1}Q_2\overline{Q_3}$$

M3S2016a

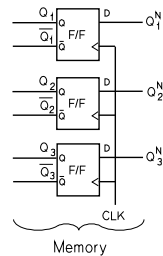
EE for EE

## *Sequential Circuit Design (Con't)*

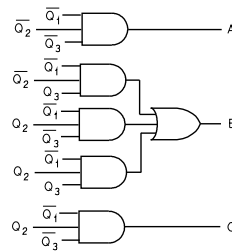
6. Draw the circuit:



\*Next State\* Logic



Memory



Output Logic

M3S2016a

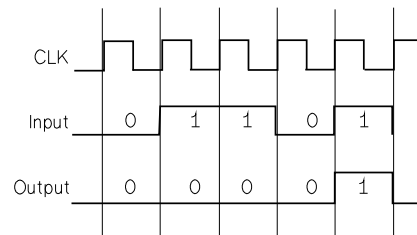
EE for EE

## Another Sequential Circuit Problem

### Sequence Detector

The problem:

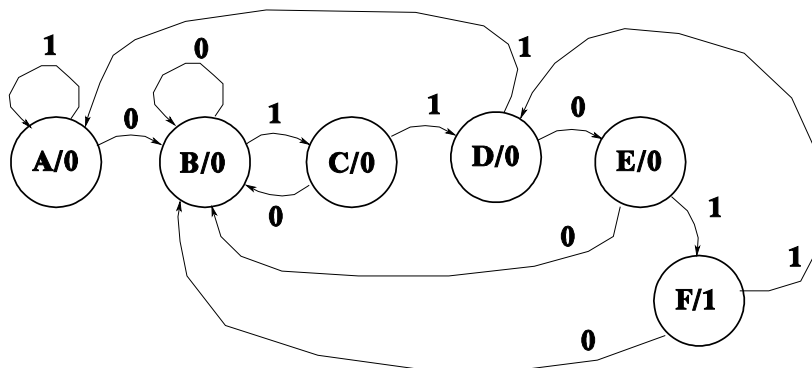
Design a circuit that will output a 1 when the following input sequence occurs:



M3S20017

EE for EE

## The State Diagram



M3S20018

EE for EE

## The Transition Table

Current State	Next State		Output
	0	1	
A	B	A	0
B	B	C	0
C	B	D	0
D	E	A	0
E	B	F	0
F	B	D	1

M3S20019

EE for EE

## State Assignment

Current State	Next State		Output
	0	1	
A-000	B-001	A-000	0
B-001	B-001	C-010	0
C-010	B-001	D-011	0
D-011	E-100	A-000	0
E-100	B-001	F-101	0
F-101	B-001	D-011	1

M3S20020

EE for EE

## Determine Next State and Output Equations

$$Q_1^N = \bar{I}\bar{Q}_1Q_2Q_3 + IQ_1\bar{Q}_2\bar{Q}_3$$

$$Q_2^N = I\bar{Q}_1\bar{Q}_2Q_3 + I\bar{Q}_1Q_2\bar{Q}_3 + IQ_1\bar{Q}_2Q_3$$

$$Q_3^N = (8 \text{ terms})$$

$$Y = Q_1\bar{Q}_2Q_3$$

M352021A

EE for EE