

CS 451 / 551 / ECE 541

ADVANCED
COMPUTER ARCHITECTURE

SESSION no. 4

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FLYNN'S TAXONOMY

SISD - CORE

SIMD -

data path pipeline

MISD -

doesn't exist

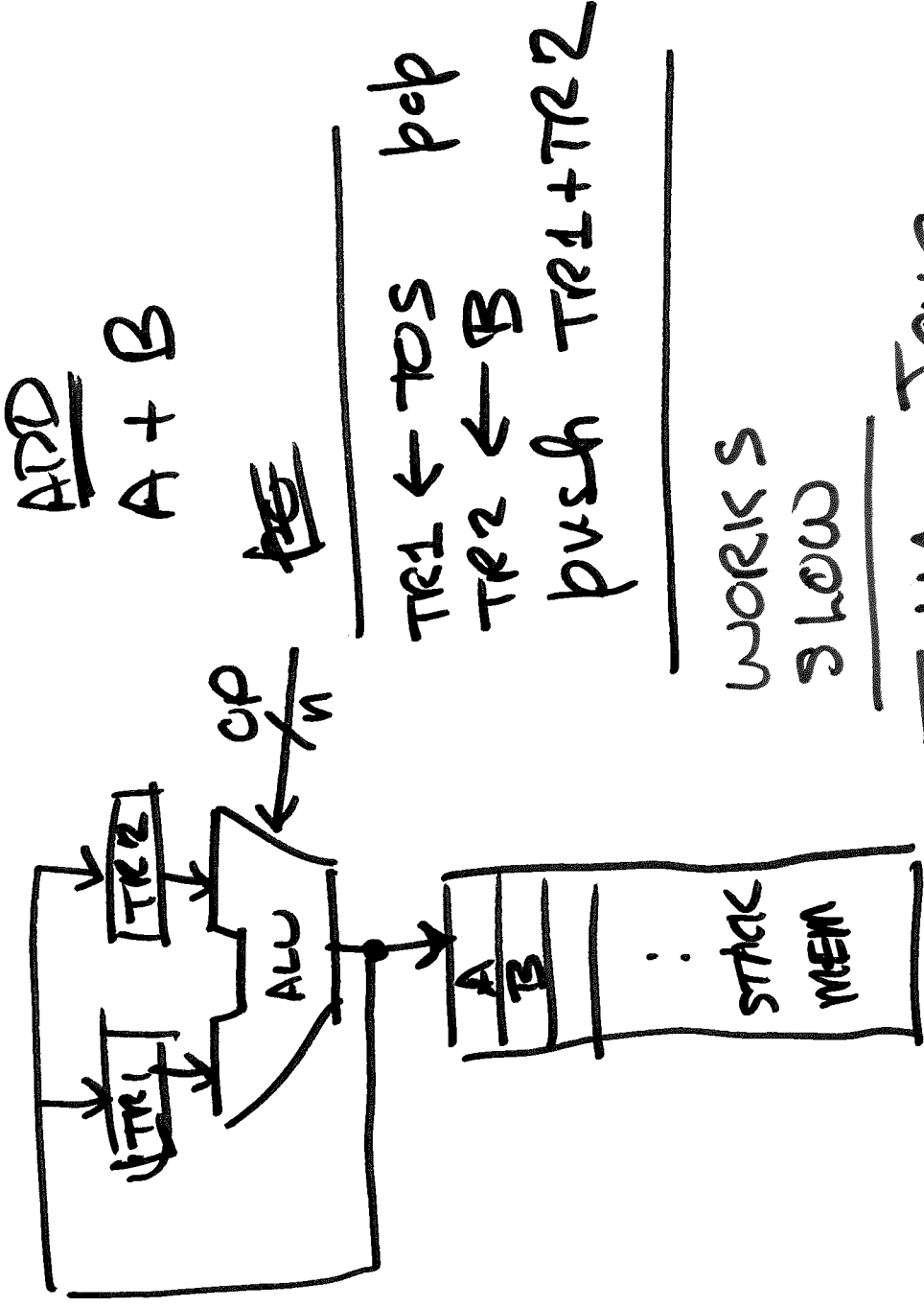
MIMD -

multi-core

Appendix A

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1. STACK ARCHITECTURE (ZERO ADDRESS)



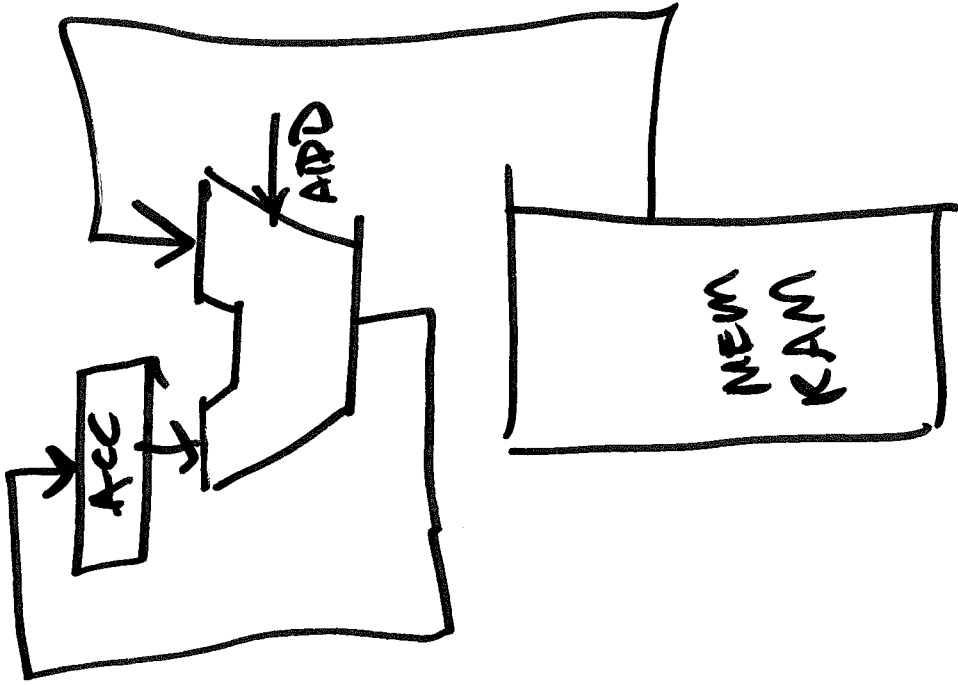
ADD
 $A + B$

$TR1 \leftarrow TOP$ pop
 $TR2 \leftarrow B$
 push $TR1 + TR2$

WORKS
SLOW

JVM - Java
Virtual Machine

2. Accumulator -



SINGLE ADDRESS

ADD MEM LOC. TO
ACC
RESULTS IN ACC

STORE - ACC TO MEM

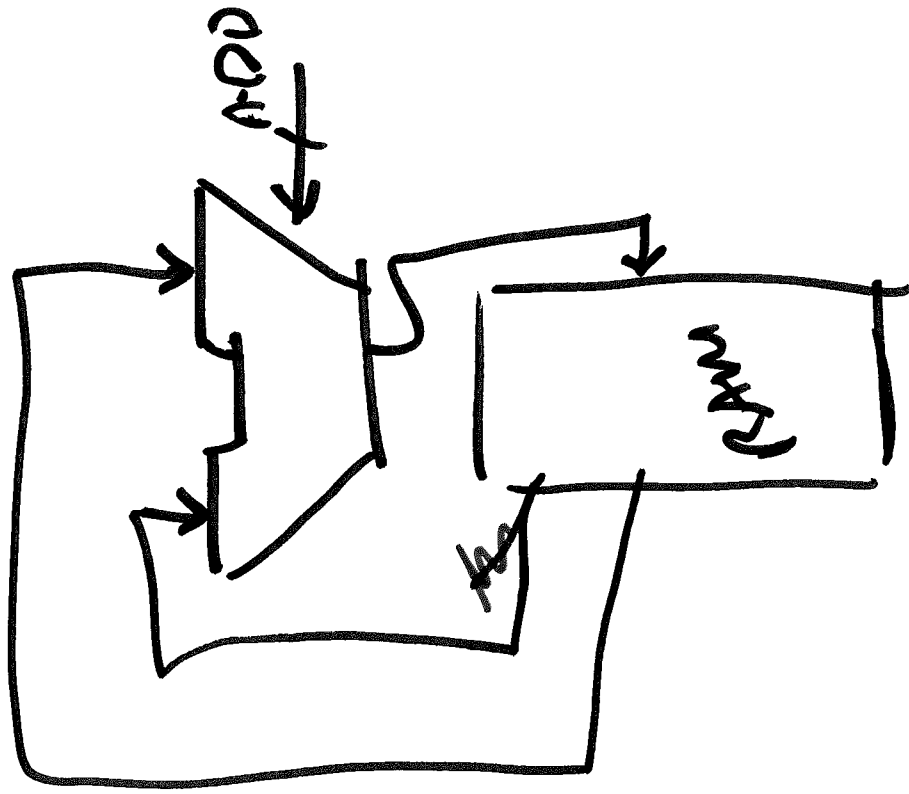
WORKS

- SLOW
- SIMPLE

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3. MEMORY TO MEMORY - 2 address

ADD MEM LOC 1 TO
MEM LOC 2, PUT
RESULT IN MEM
LOC 3.



4. REGISTER TO REGISTER

OP - ADD,
AND...

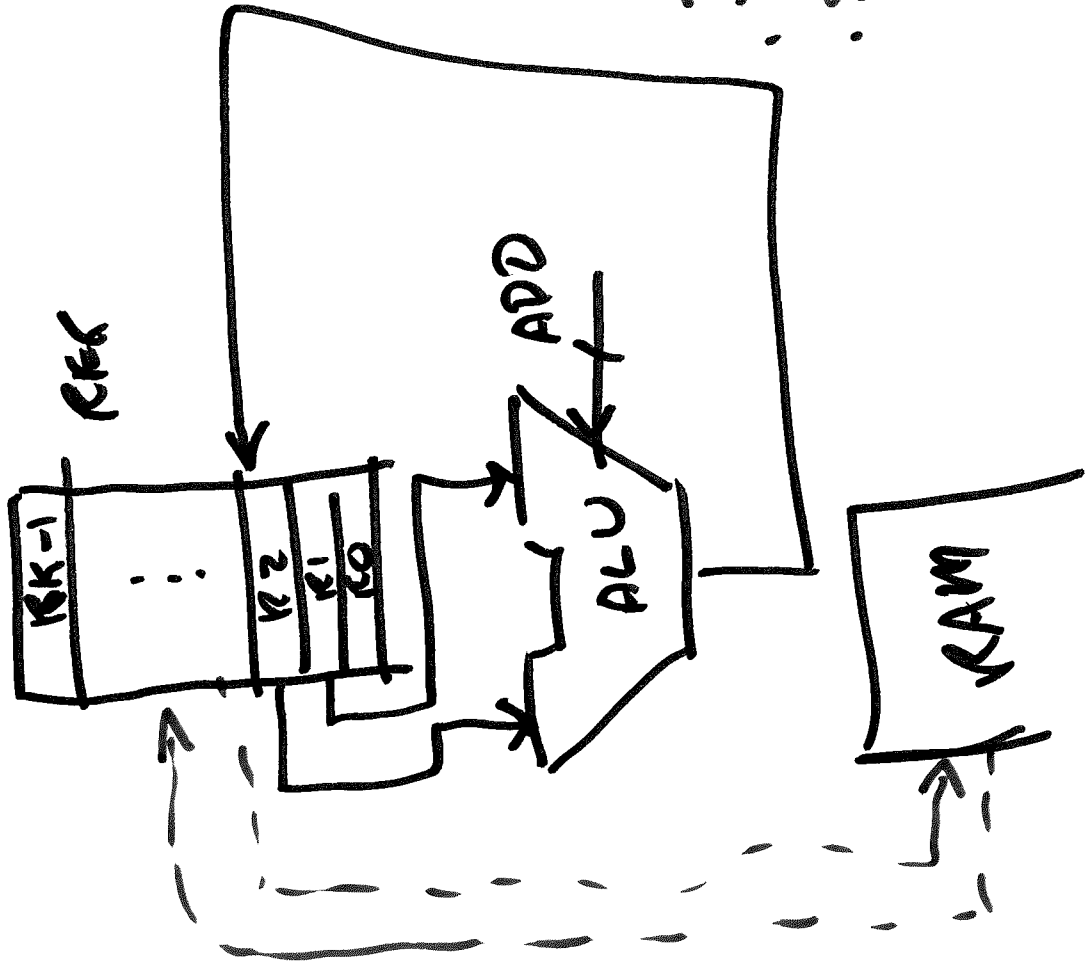
LOAD -
MEM → REG

STORE -
REG - MEM

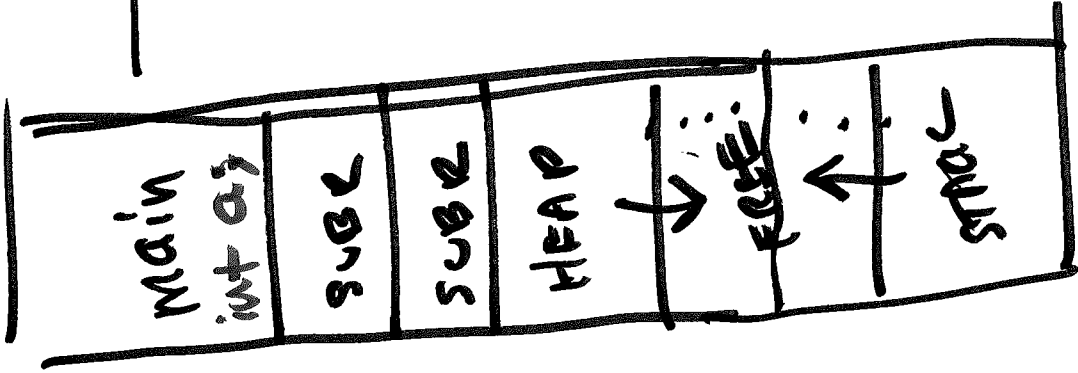
REGISTERS

FAST

SMALL



MEMORY MODEL



DATA

TEXT / SYMBOLS

ASCII
UNICODE

FLOAT

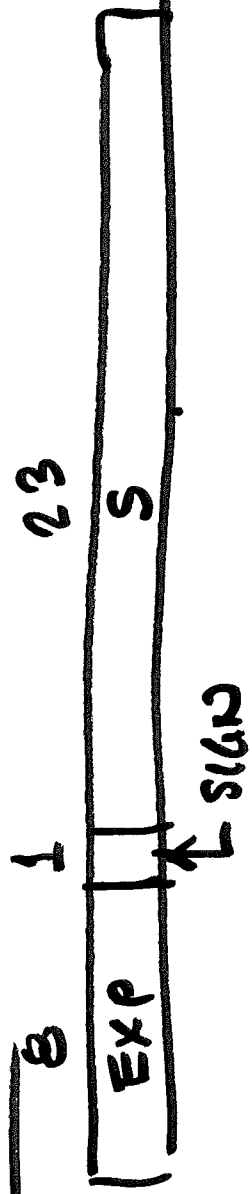
"real"
quantities
Sci
modeling

INTEGERS

Numbers
pixels, color
addresses

Fixed
range
n-bits
unsigned $[0, 2^{n-1}]$
signed $[-2^{n-1}, 2^{n-1}]$

Float



Value = $S \times 2^{\text{EXP}}$ IEEE

SINGLE PRECISION: $|2^{23} \times 2^7|$ - 32 bits

MAX = BIG!

DB = 11 + 1 + 52 - 64 bits.

MAX = REALLY BIG!

ALSO

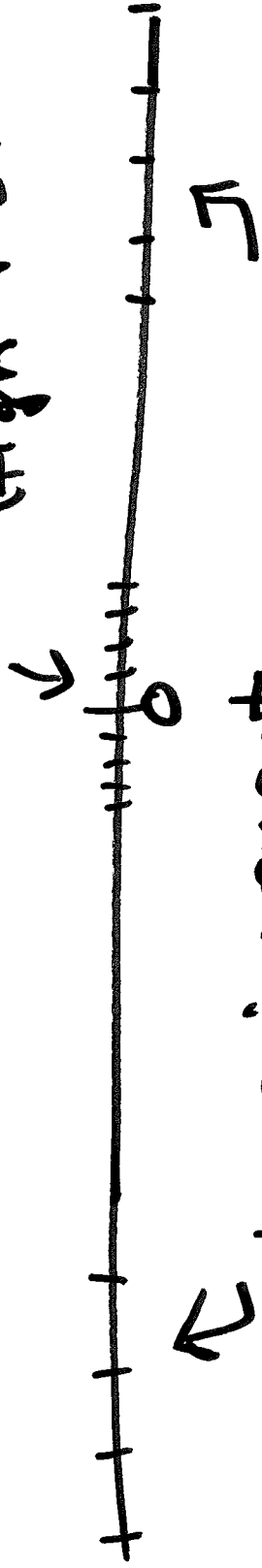
∞ , $-\infty$, NaN

TRIGGER EXCEPTIONS!
NOT A NUMBER!

FLOAT. TRADE RANGE FOR RESOLUTION

$$S \times 2^E N$$

small increments
high res.



FP is expensive

- SOFTWARE 20-30x as much code as integer
- HARDWARE chip area
- Power PC $\frac{1}{6}$ area = FP U

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- SPECIFIC FLOATING POINT
- INSTRUCTIONS
- REGISTERS

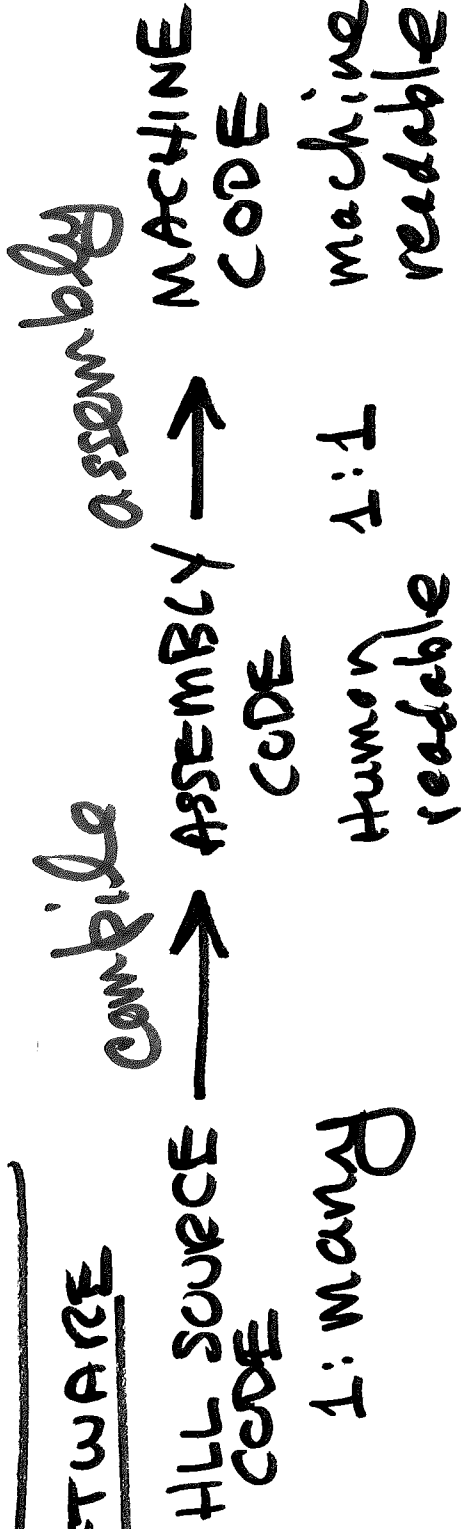
- SPEC -
INTEGER VERSIONS
F.P. VERSIONS

MIPS architecture

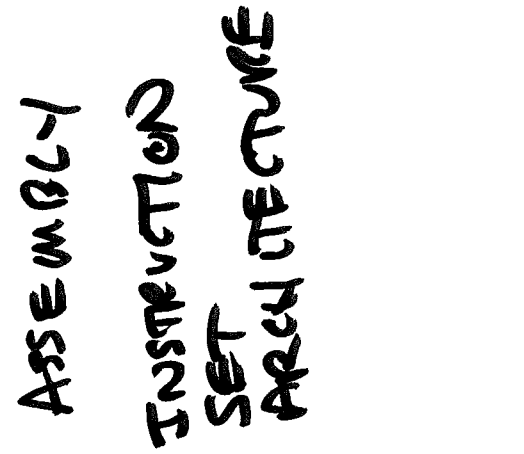
- Open source
- Descendants - ARM
- Most popular processor
- iPhones, ~~tablets~~ tablets

NOTATION

SOFTWARE



HARDWARE



ASSEMBLY

RTL

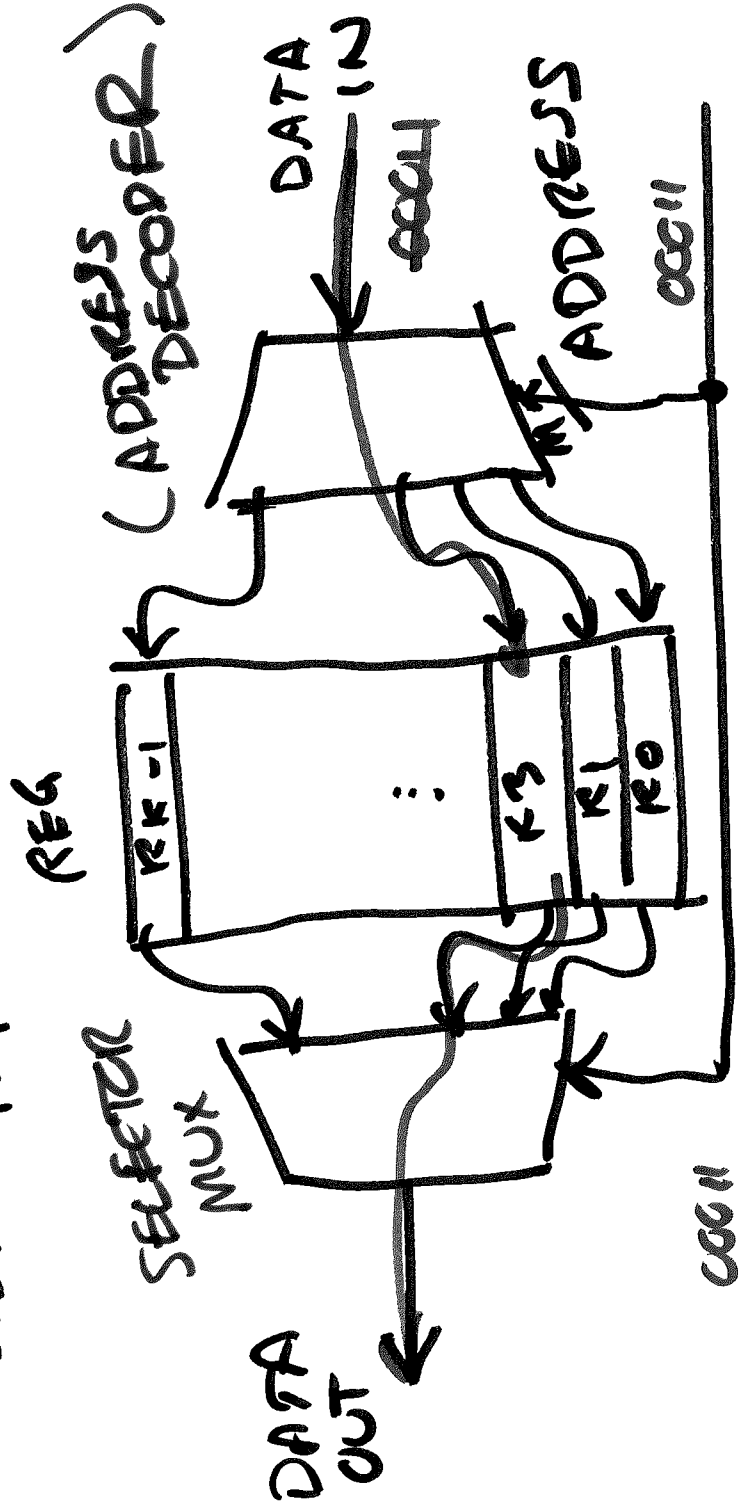
ADD R4, R3 REGS[R4] ← REGS[R3] +

SR1 = R4

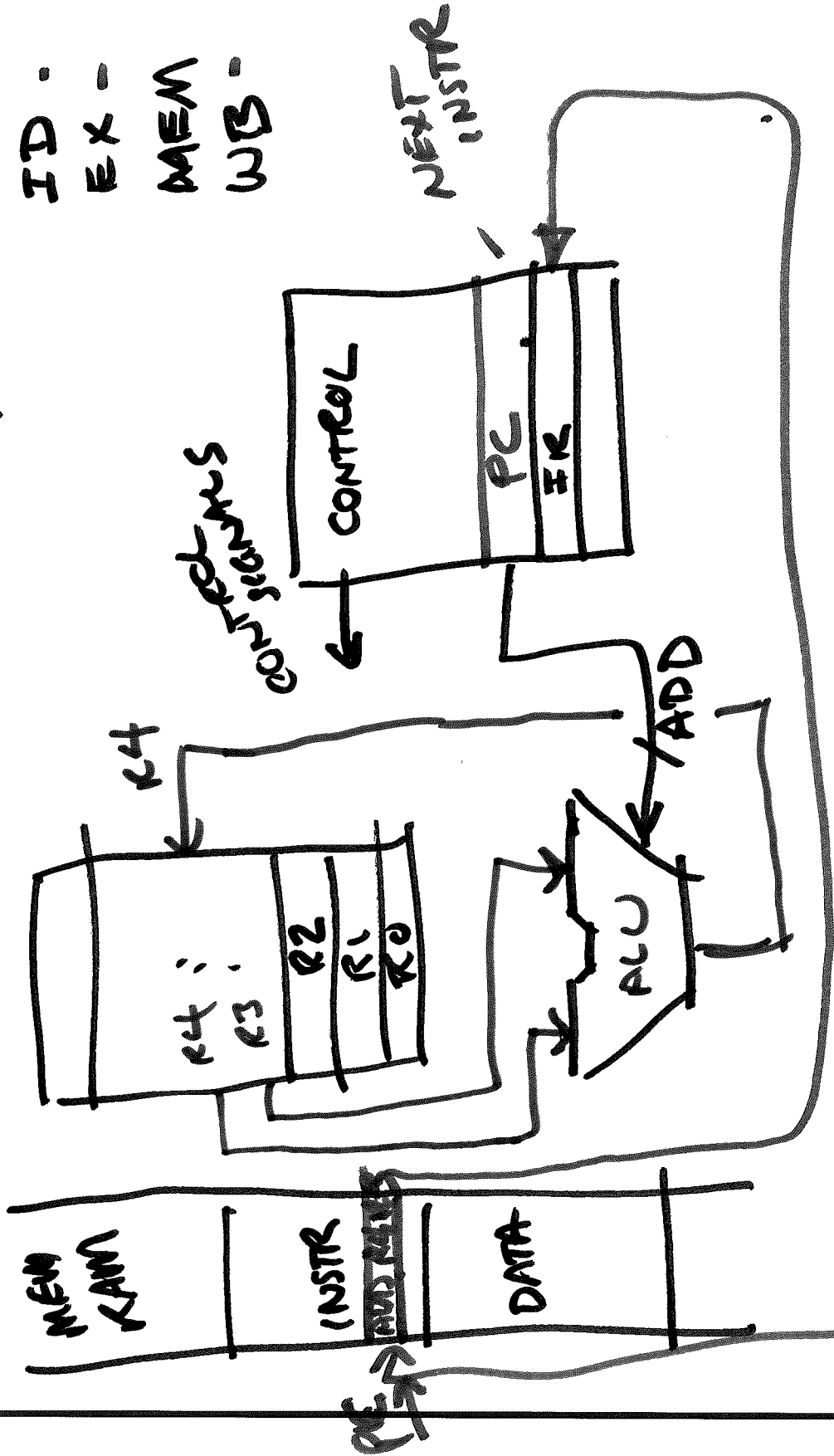
SR2 = R3

DEST = R4

REGS[R3]



ADD R4, R3
 IF -
 ID -
 EX -
 MEM
 WB -

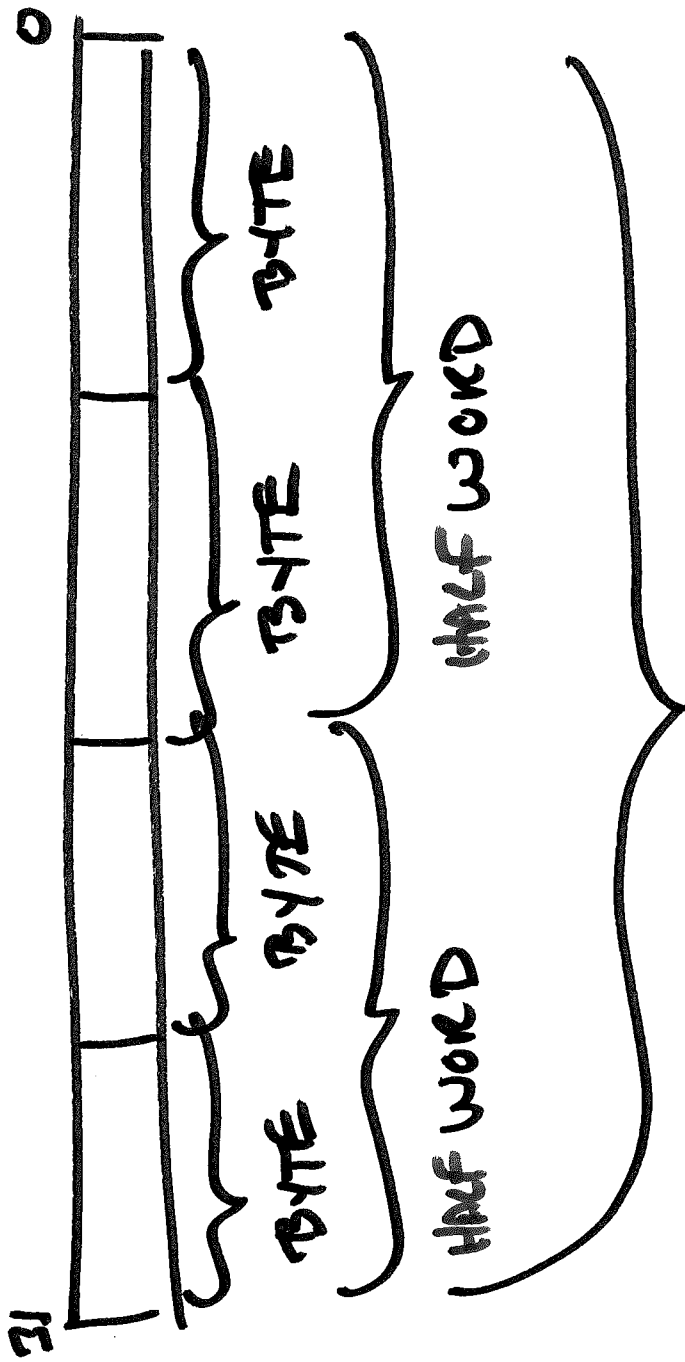


ADD R4, R3
 IR = INSTRUCTION REG

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DATA ADDRESSING

MIPS 32 WORDS ARE 32 BITS



~~LONG WORD~~

LOAD & STORE

