

CS 451 / 551 / ECE 541

ADVANCED
COMPUTER ARCHITECTURE

SESSION no. 11

University of Idaho

OPTOELECTRONIC INTERCONNECT?

• METAL INTERCONNECT A BOTTLENECK?

• WHY LIGHT?

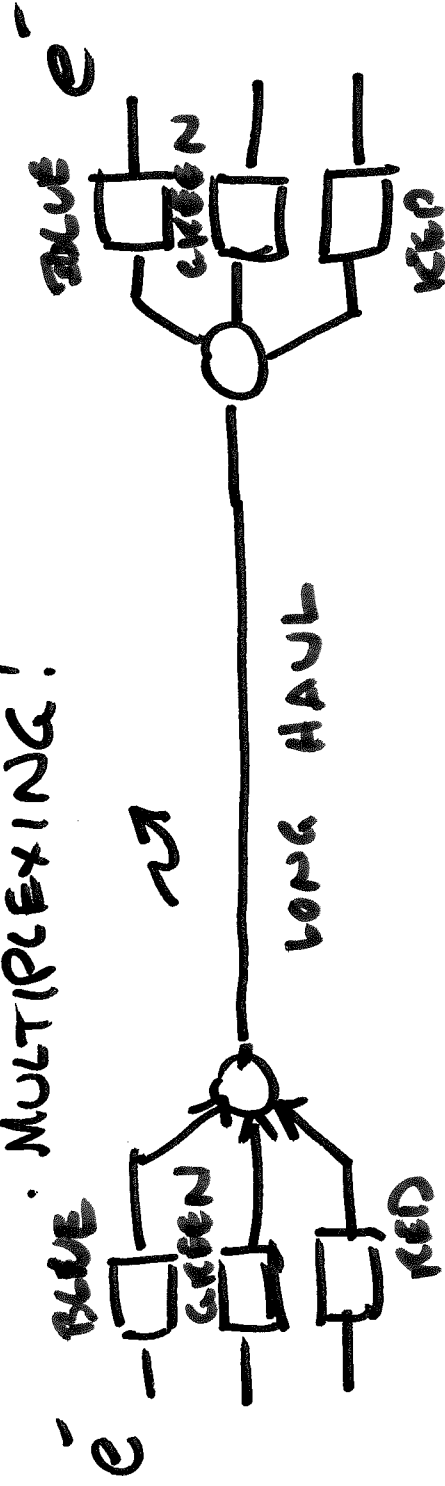
WIRES -

- PROPAGATION $\approx \frac{1}{2}$ SPEED OF LIGHT
- SWITCHING SPEED: ≈ 1 GHz

OPTICAL -

- LARGE BANDWIDTH POSSIBLE

• MULTIPLEXING!



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• ALTERNATIVES VON NEUMANN COMPUTER

FOR:

- FACIAL RECOGNITION
- MACHINE LEARNING
- NEURAL NETWORK?

ARE CURRENT TECHNOLOGIES INAPPROPRIATE?

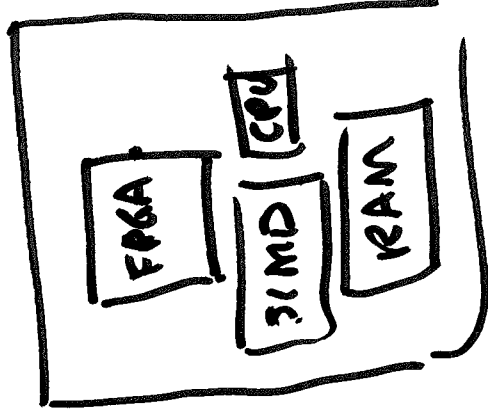
1. RECONFIGURABLE ~~COMPUTER~~ COMPUTING!

PROGRAMMABLE SYSTEM-ON-A-CHIP

- FPGA LOGIC FABRIC
- SIMD DSP CHAINS
- CPUs
- MEM

MUCH DESIGN EFFORT!

VHDL, ...



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2. MULTICORE - GPGPU

- 100's OF GP PROCESSORS
- VECTER, SIMD
- C/S, THREADS
- C-FAMILY (CUDA)

UNDER-EXPLOITED!

BOARD - \$500

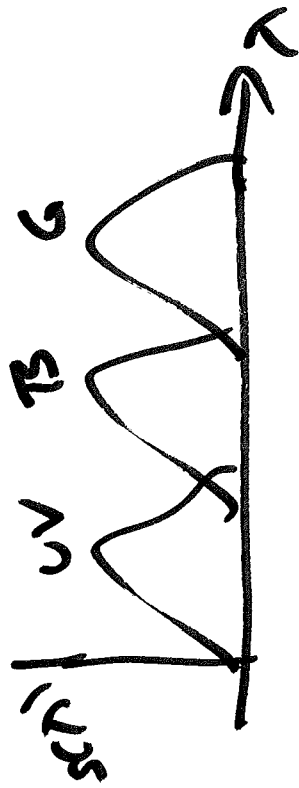
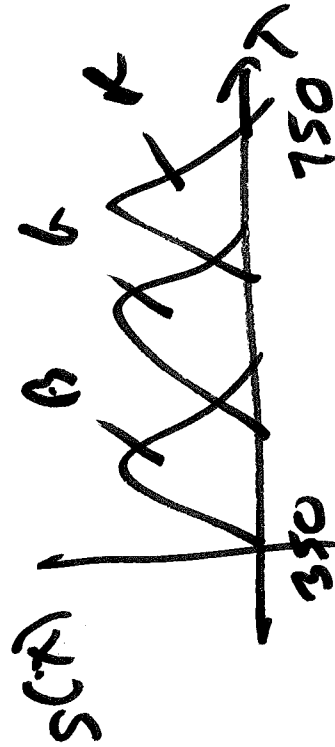
BEOWULF - \$500,000

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ARTIFICIAL NEURAL NETWORKS



HUMAN



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ARTIFICIAL NEURAL NETWORKS

CS 578

BIOMIMETIC MODELS FOR

COMPUTATION

GARTNER GROUP

ANN HYPE CYCLE

PEAK OF UNREALISTIC EXPECTATIONS

PLATEAU OF PRODUCTIVITY

SCOPE OF

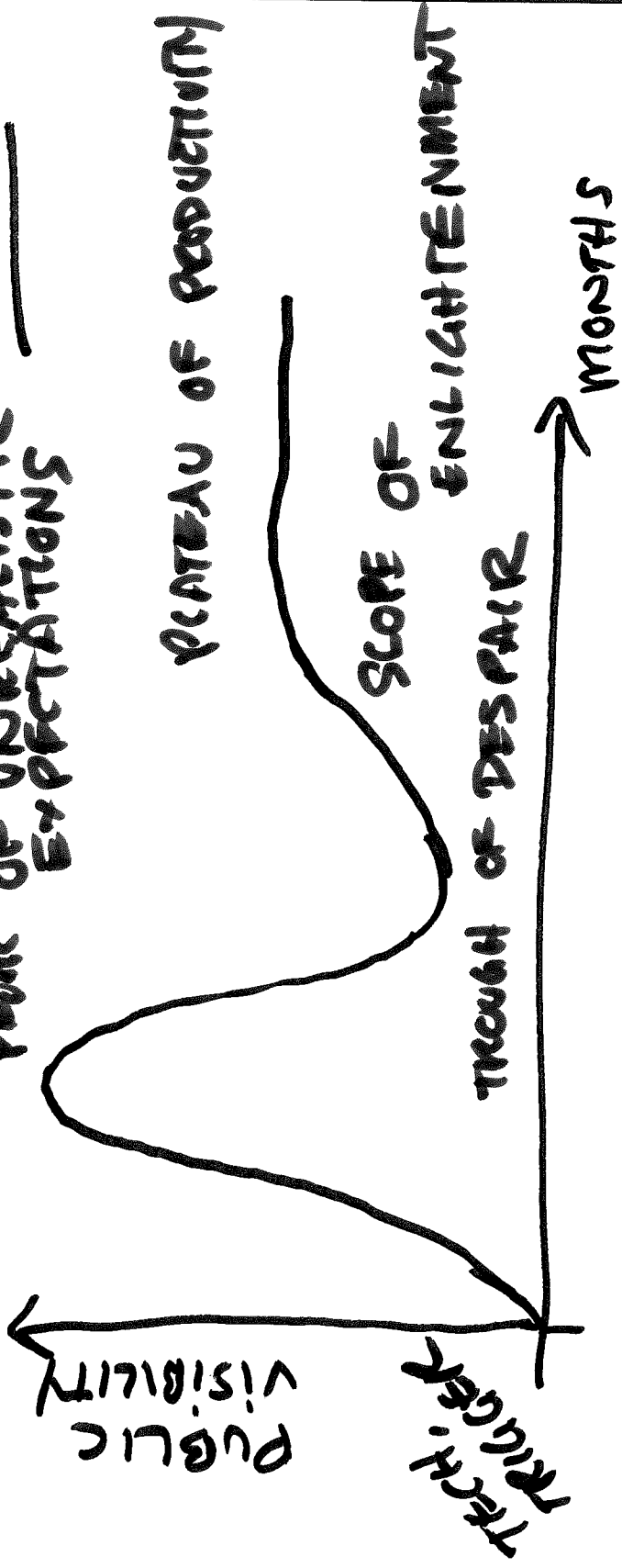
ENLIGHTENMENT

TROUGH OF DESPAIR

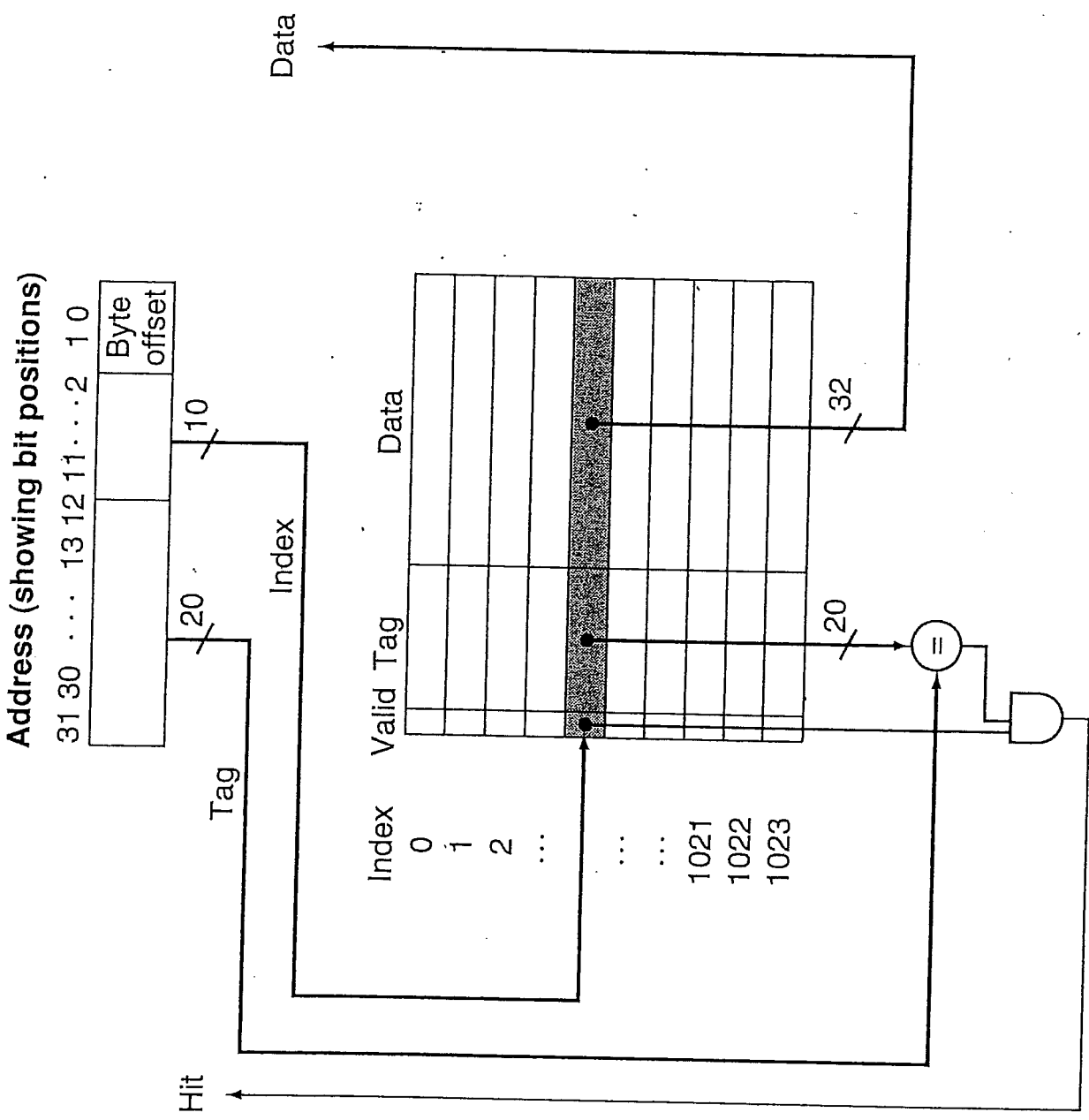
MONTHS

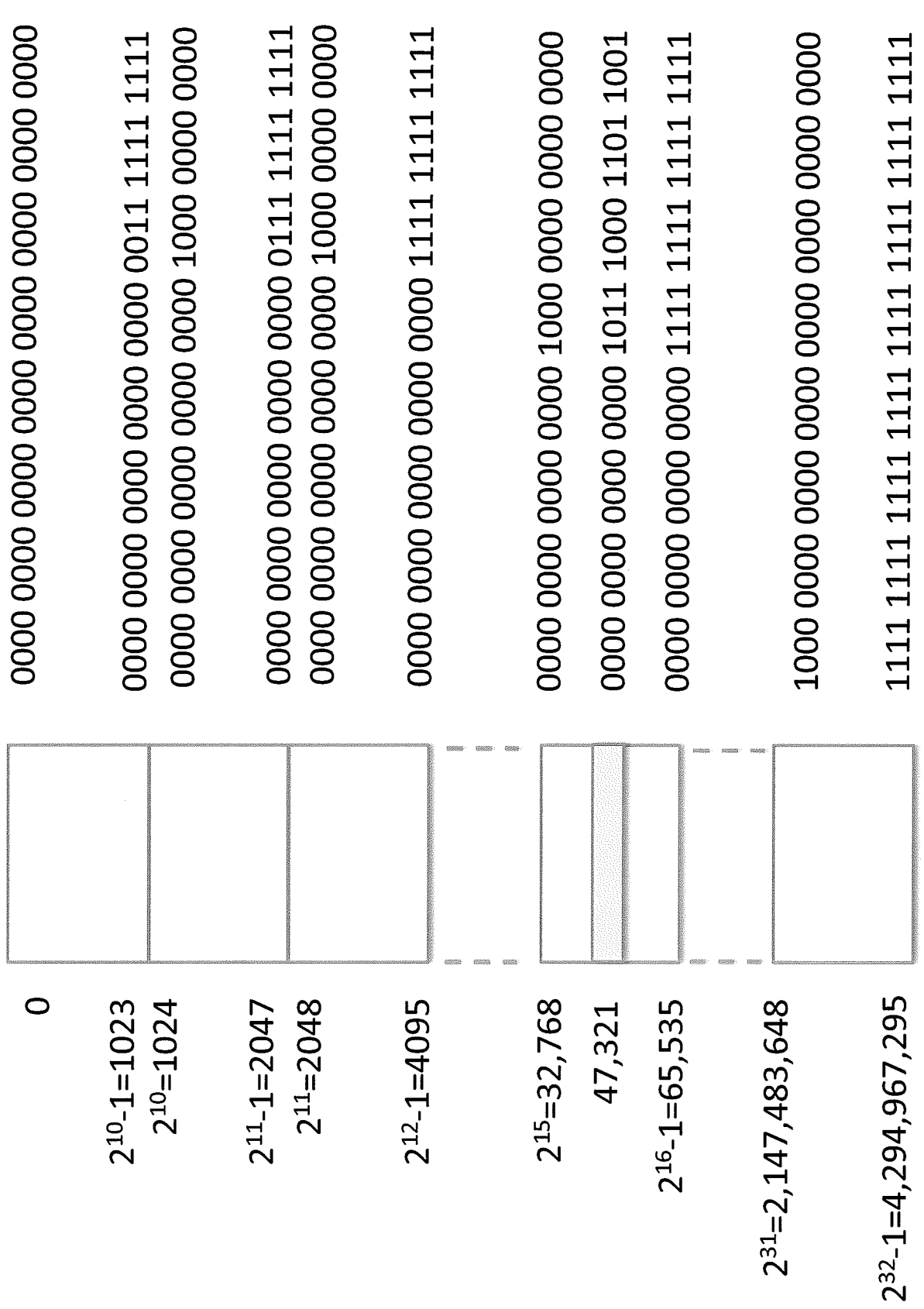
PUBLIC VISIBILITY

TRIGGER



7





ADDR = 47321₁₀

0000 0000 0000 0000	1011 1000	1101 1001
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Tag Index Byte

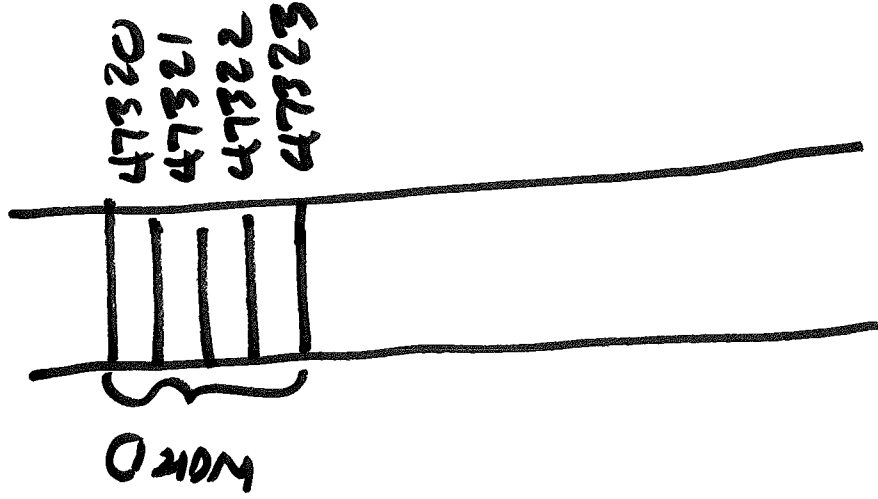
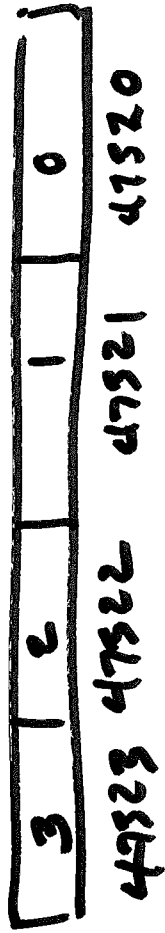
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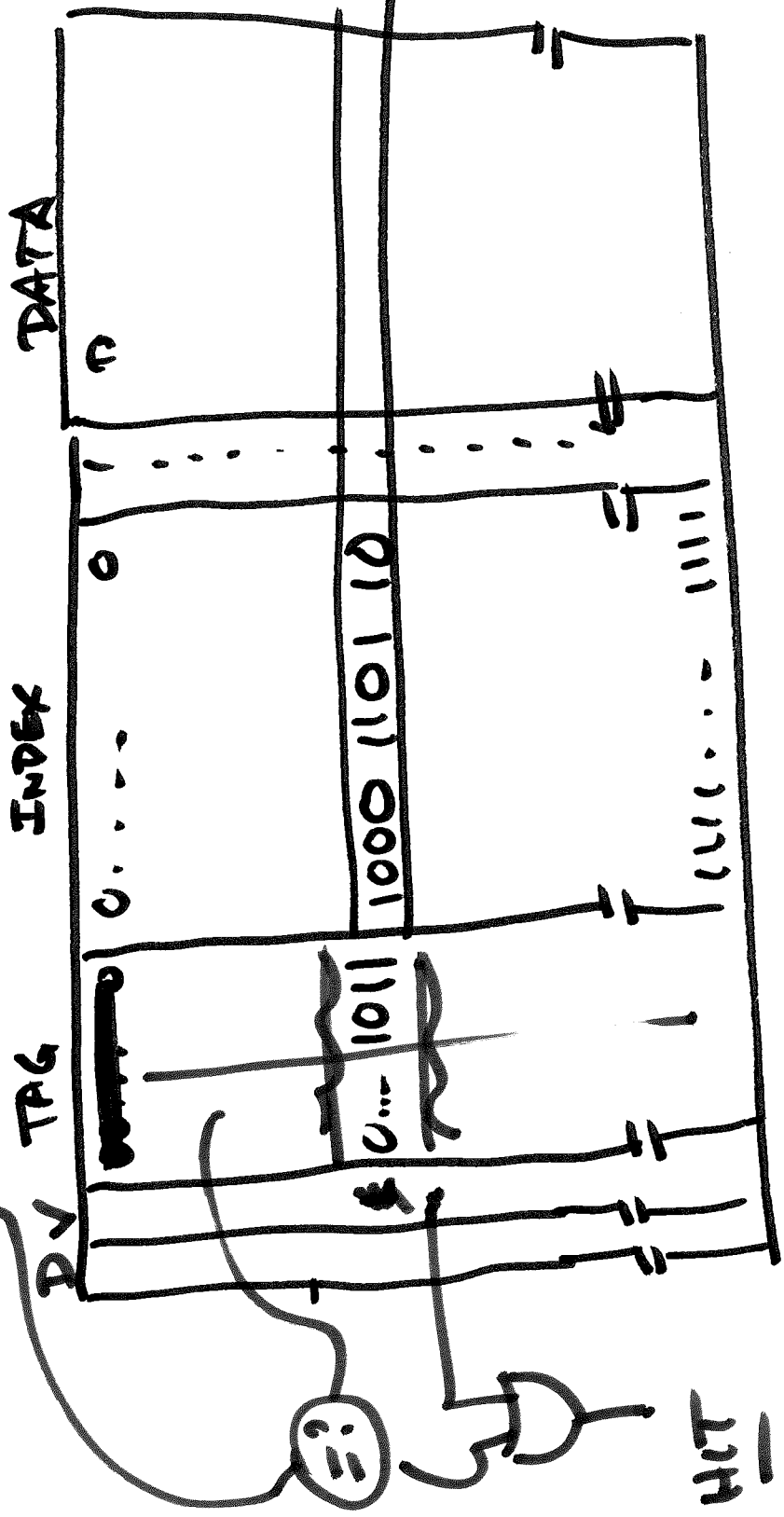
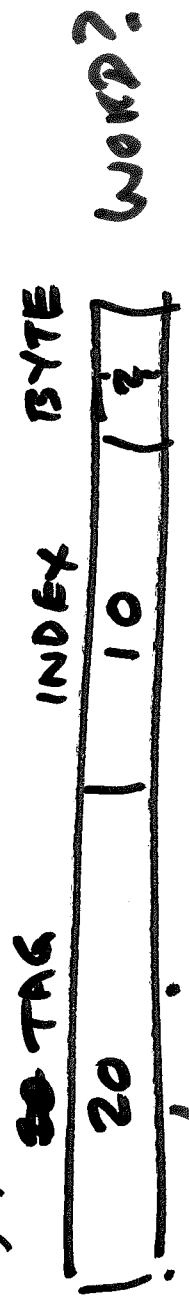
DIRECT-MAPPED CACHE

- cpu
 - REG
 - |
 - CACHE
 - |
 - MEM
 - |
 - BUK
 - :
 - :
- BLOCKS OF MEMORY
 - ONE BLOCK AT A TIME INTO CACHE
 - WHEN DONE,
 - WRITE OUT BLOCK TO MEM (IF IT CHANGED)
 - OVERLAY CACHE WITH A NEW BLOCK

BYTE ADDRESSABLE

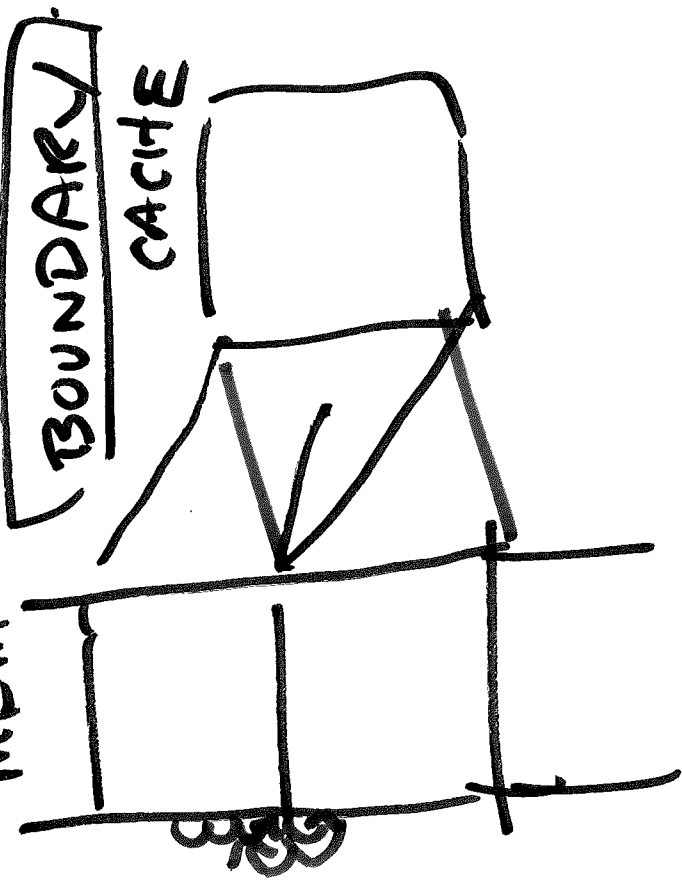
WORD = 32 BITS





IS WORD IN CACHE? IS BLOCK IN CACHE?

MEM

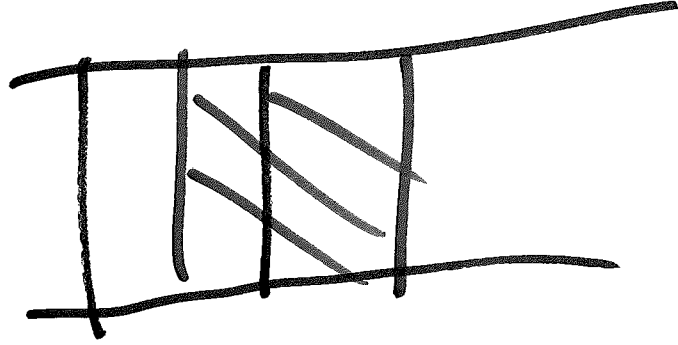


DIRECT MAPPED

EXCESSIVE
CACHE MISSES

ASSOCIATIVE CACHE (FULLY)

• BLOCK NOT RESTRICTED TO FIXED BOUNDARIES.



IS MEM ITEM IN CACHE?

- CHECK ALL LOCATIONS
- CONTENT - ADDRESSABLE MEMORY

ADDRESS ASSOCIATE WITH
CACHE ENTRY.

ASSOCIATIVE ARRAY

CHORES = { BILL: DISHES,
 ALICE: IRONING,
 BOB: GARBAGE }

CHORES[ALICE] = IRONING

CHORES[1] = IRONING