

CS 451/551+ECE541

Advanced Computer Architecture

Fall 2013

Catalog Description: Principles and alternatives in instruction set design; processor implementation techniques, pipelining, parallel processors, memory hierarchy, and input/output; measurement of performance and cost/performance trade-off.

Total Credits: 3

Instructor: Gregory W. Donohoe

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Office Hours: TBD

Class Location: JEB 025

Class Day and Time: Tues-Thurs, 11:00 AM– 12:15 PM

Prerequisites:

- CS 150: Computer Organization and Architecture, or equivalent
- Stat 301: Probability and Statistics, or equivalent

URL: http://www2.cs.uidaho.edu/~cs451_551/

Prereq: CS 150, Stat 301, or permission

Textbook: John Hennessy and David Patterson, *Computer Architecture - A Quantitative Approach*, 4rd Ed, Morgan Kaufmann, 2006, or equivalent text.

Major Topics Covered

- Pipelining concepts
- Instruction-level parallelism
- Dynamic scheduling
- Limits on ILP
- Exploiting ILP with software
- Memory hierarchy and caches
- Virtual memory
- Memory performance optimization
- Multiprocessors - thread level parallelism
- Storage systems
- Interconnection networks and clusters

Course Outcomes

At the conclusion of this course, the student should be able to:

- Classify processors by architecture type
- Describe how memory cache functions
- Analyze the tradeoffs in cache design, and select an optimal design for a particular application
- Understand the issues and tradeoffs in instruction pipelining
- Understand non-pipelined instruction-level parallelism, e.g. Tomasulo's algorithm
- Understand and describe practical issues in parallel computing, such as
 - Thread-level parallelism
 - Cache coherence
- Analyze input/output devices for performance: interconnection networks, redundant array of independent disks (RAID).

Grading

	CS 451/ECE 441	CS 551/ECE 541
Two in-class exams	50%	40%
Final exam	25%	20%
Assignments	25%	15%
Term project		25%
Total	100%	100%