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- Boeing 777 Primary Flight Computer
  - Paper: *Triple-Triple Redundant 777 Primary Flight Computer*
    - Y.C. Yeh
    - 1996 IEEE Aerospace Applications Conference
    - pg 293-307

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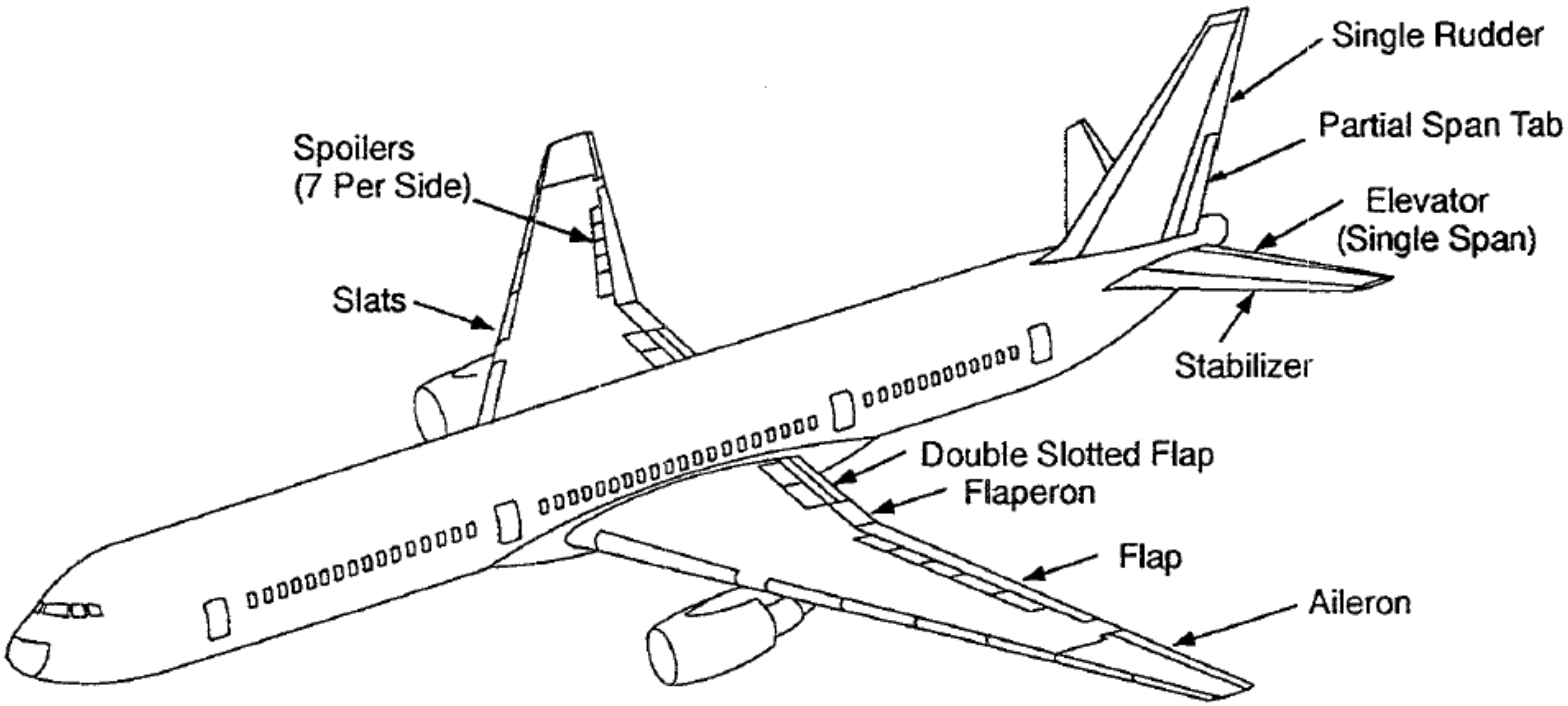
– Primary Flight Control Surfaces



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- Overview
  - Flight control system is a *Fly-by-Wire* (FBW) system.
  - Delayed Maintenance for major electronic Line Replacement Units (LRU)
  - Triple redundancy for all hardware
    - computing system
    - airplane electrical power
    - hydraulic power
    - communication paths
  - Primary Flight Computer (PFC) are the central computational elements of the FBW system.
  - PFC architecture is based on TMR

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- N-version dissimilarity integrated into TMR
  - 3 similar channels
  - each channel has 3 dissimilar computation lanes
  - software written in ADA (dissimilar compilers)
- DATAC bus, also known as ARINC 629 bus, is used for all communication between all computing systems for flight control functions.
  - DATEC = Digital Autonomous Terminal Access Communication
  - designed by Boeing
  - busses are isolated (physically and electrically)
  - DATACs are not synchronized
  - http://www.arinc.com

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- 777 FBW design philosophy
  - Considerations
    - common mode/common area fault
    - separation of FBW components
    - FBW functional separation
    - dissimilarity
    - FBW effect on the structure
  - Triple-dissimilarity for PFC processors and interface hardware
  - By nature of TMR no Byzantine faults allowed.
  - Avoidance of asymmetry by:
    - ARINC629 requirements
    - Deal with root causes of functions/communication asymmetry

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- Flight Control Functions
  - Control electric and electro-hydraulic actuators
  - Provide manual and automatic control in pitch, roll and yaw axes
  - Control pilot input: column, wheel, rudder pedals, speed brakes
  - Pitch Control: 2 elevators and horizontal stabilizer
  - Roll Control: 2 ailerons, 2 aperons, 14 spoilers
  - Jaw Control: tabbed rudder

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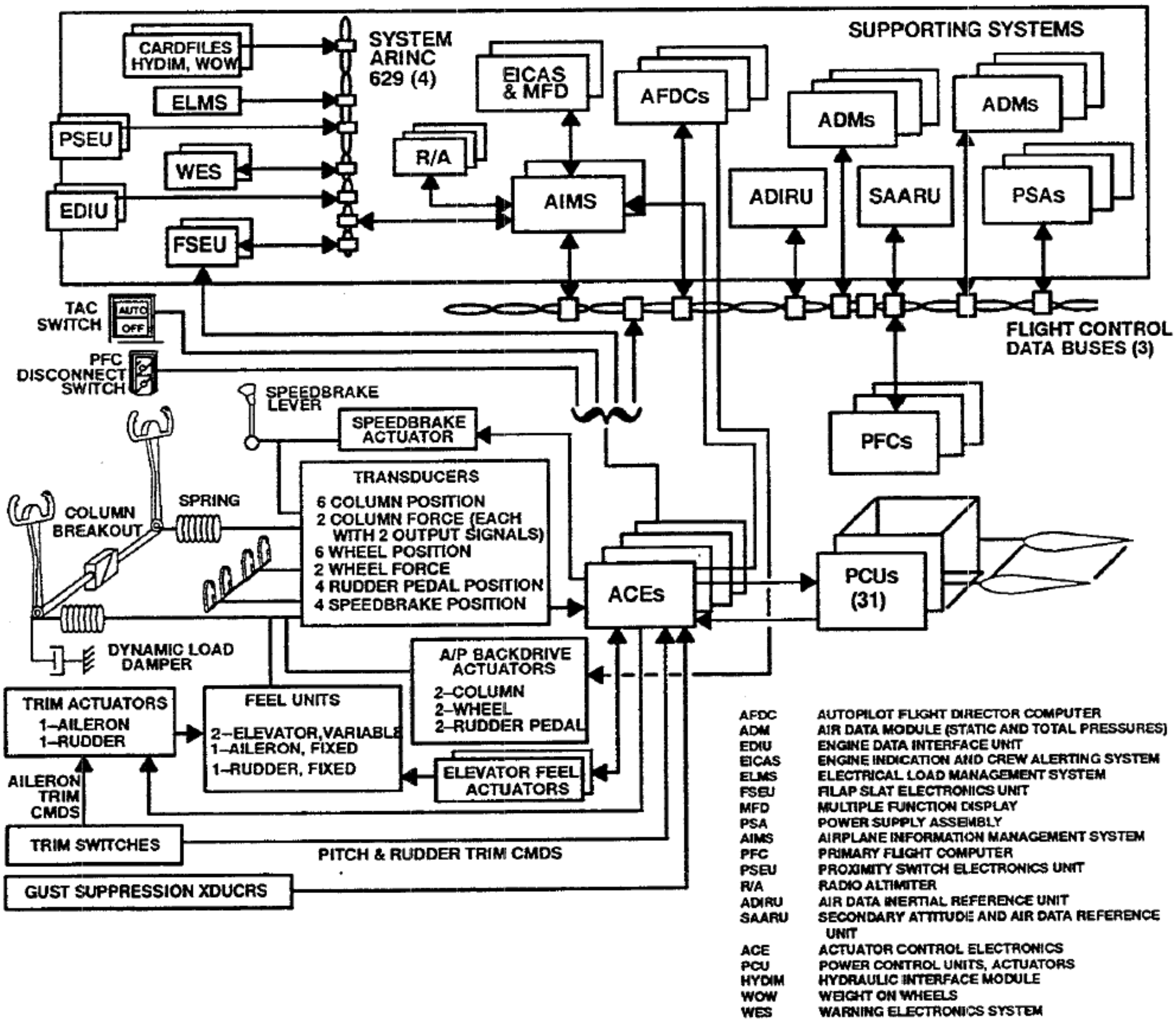
- Three operation modes:

Table 1 777 Primary Flight Control Modes

CONTROL MODE	PITCH	ROLL	YAW
NORMAL CONTROL	CONTROL C* Maneuver Cmd with Speed Feedback Manual Trim for Speed Variable Feel ENVELOPE PROTECTION Stall Overspeed AUTOPILOT Backdrive	CONTROL Surface Cmds Manual Trim Fixed Feel ENVELOPE PROTECTION Bank Angle AUTOPILOT Backdrive	CONTROL Surface Cmd Ratio Changer Wheel/Rudder Cross Tie Manual Trim Yaw Damping Fixed Feel Gust Suppression ENVELOPE PROTECTION Thrust Asymmetry Compensation AUTOPILOT Backdrive
SECONDARY CONTROL	CONTROL Surface Cmd (Augmented) Flaps Up/Down Gain Direct Stabilizer Trim Flaps Up/Down Feel	CONTROL Surface Cmd Manual Trim Fixed Feel	CONTROL Surface Cmds, Flaps Up/Down Gain PCU Pressure Reducer Manual Trim Fixed Feel Yaw Rate Damper (If Available)
DIRECT CONTROL	CONTROL Surface Cmd (Augmented) Flaps Up/Down Gain Direct Stabilizer Trim Flaps Up/Down Feel	CONTROL Surface Cmd Manual Trim Fixed Feel	CONTROL Surface Cmds, Flaps Up/Down Gain PCU Pressure Reducer Manual Trim Fixed Feel


SUPPORTING SYSTEMS
CARDFILES HYDIM, WOW
ELMS
PSEU
WES
EDIU
FSEU
SYSTEM ARINC 629 (4)
EICAS & MFD
R/A
AIMS
AFDCs
ADMs
ADIRU
SAARU
ADMs
PSAs
TAC SWITCH
AUTO
OFF
PFC DISCONNECT SWITCH
FLIGHT CONTROL DATA BUSES (3)
SPEEDBRAKE LEVER
SPEEDBRAKE ACTUATOR
PFCs
COLUMN BREAKOUT
SPRING
TRANSDUCERS
6 COLUMN POSITION
2 COLUMN FORCE (EACH WITH 2 OUTPUT SIGNALS)
6 WHEEL POSITION
2 WHEEL FORCE
4 RUDDER PEDAL POSITION
4 SPEEDBRAKE POSITION
ACEs
PCUs (31)
DYNAMIC LOAD DAMPER
A/P BACKDRIVE ACTUATORS
2–COLUMN
2–WHEEL
2–RUDDER PEDAL
TRIM ACTUATORS
1–AILERON
1–RUDDER
FEEL UNITS
2–ELEVATOR, VARIABLE
1–AILERON, FIXED
1–RUDDER, FIXED
ELEVATOR FEEL ACTUATORS
AILERON TRIM CMDS
TRIM SWITCHES
PITCH & RUDDER TRIM CMDS
GUST SUPPRESSION XDUCRS
AFDC AUTOPILOT FLIGHT DIRECTOR COMPUTER
ADM AIR DATA MODULE (STATIC AND TOTAL PRESSURES)
EDIU ENGINE DATA INTERFACE UNIT
EICAS ENGINE INDICATION AND CREW ALERTING SYSTEM
ELMS ELECTRICAL LOAD MANAGEMENT SYSTEM
FSEU FLAP SLAT ELECTRONICS UNIT
MFD MULTIPLE FUNCTION DISPLAY
PSA POWER SUPPLY ASSEMBLY
AIMS AIRPLANE INFORMATION MANAGEMENT SYSTEM
PFC PRIMARY FLIGHT COMPUTER
PSEU PROXIMITY SWITCH ELECTRONICS UNIT
R/A RADIO ALTIMETER
ADIRU AIR DATA INERTIAL REFERENCE UNIT
SAARU SECONDARY ATTITUDE AND AIR DATA REFERENCE UNIT
ACE ACTUATOR CONTROL ELECTRONICS
PCU POWER CONTROL UNITS, ACTUATORS
HYDIM HYDRAULIC INTERFACE MODULE
WOW WEIGHT ON WHEELS
WES WARNING ELECTRONICS SYSTEM

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Sequence of events:

1) Actuator Control Electronics unit (ACE)

- Position transducers (mounted on each pilot controller) sense pilot commands for the ACE
  - » two actuator controlled feel units provide variable feel for control column
  - » mechanical feel units provide fixed feel for wheel and paddles.
- ACE performs A/D conversion
- Transmits signals to PFCs via redundant ARINC 629 buses

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2) Primary Flight Computer

- Receive inertial data from
  - Air Data Inertial Reference System (ADIRS)
  - Secondary Attitude and Air Data Reference Unit (SAARU)
  - ACE
- Compute Control-Surface position commands
- Transmit position commands back to ACE via ARINC 629 buses

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3) Actuator Control Electronics unit

- Receives digital command from PFC
- D/A conversion
- Control electro-hydraulic actuators of control surfaces
- In *Direct Mode*, the ACEs use the analog pilot controller transducer signals to generate surface commands

◆ Line Replacement Unit (LRU)

- PFC and ACE are the major LRU, connected via ARINC 629 buses

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- Actuator Control Electronics (ACE)
  - 4MR configuration
  - Interface between analog domain, e.g. crew controllers, electric/ electro-hydraulic actuators, and digital domains, e.g. ARINC 629, PFCs
  - Controls all control surfaces
  - Controls variable feel actuators
  - 3 ARINC 629 interfaces
  - In *Direct Mode* commands on the digital bus are ignored => Provide direct surface control

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Yeh96 fig. 3

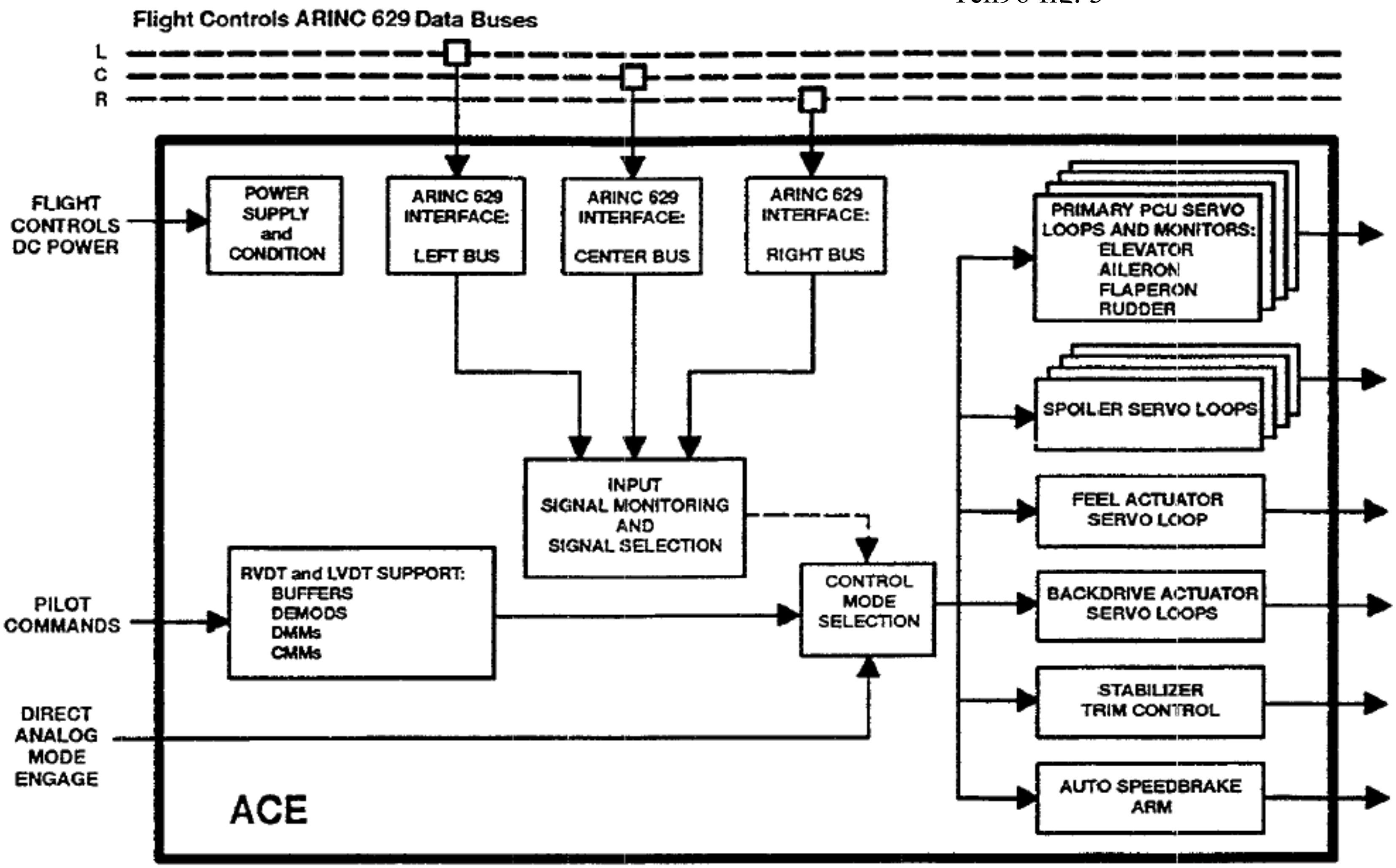

Figure 3 Actuator Control Electronics Overview

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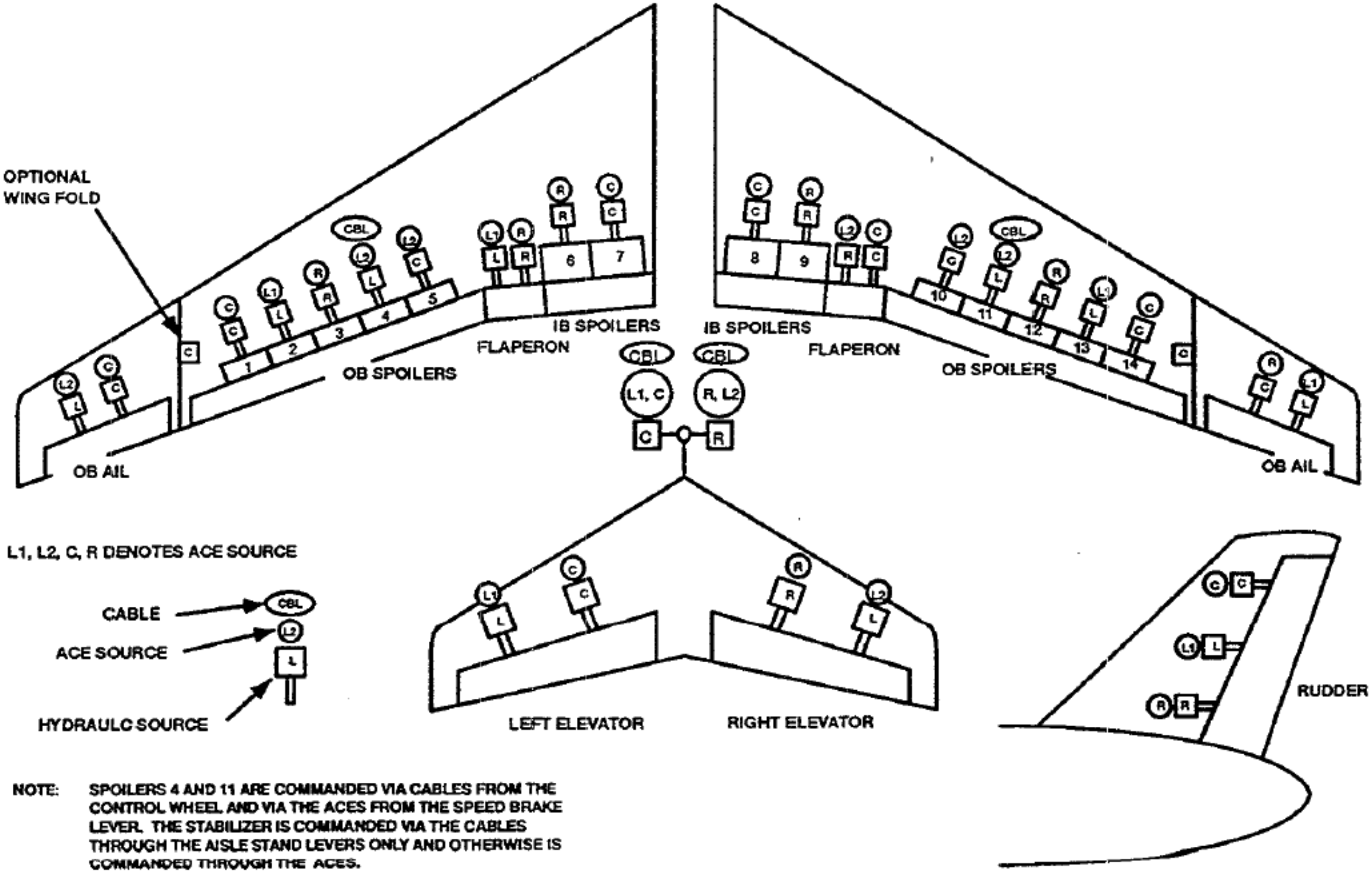

Figure 4 777 Primary Flight Controls Hydraulic / ACE Distribution

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- Primary Flight Computer (PFC)
  - TMR configuration
  - Receive data on all 3 ARINC 629 buses
  - Transmit on only one ARINC 629 bus
  - Each PFC contains 3 internal computation lanes
  - Each lane accesses all 3 buses
  - Each lane has dissimilar processors
  - Different Ada compilers

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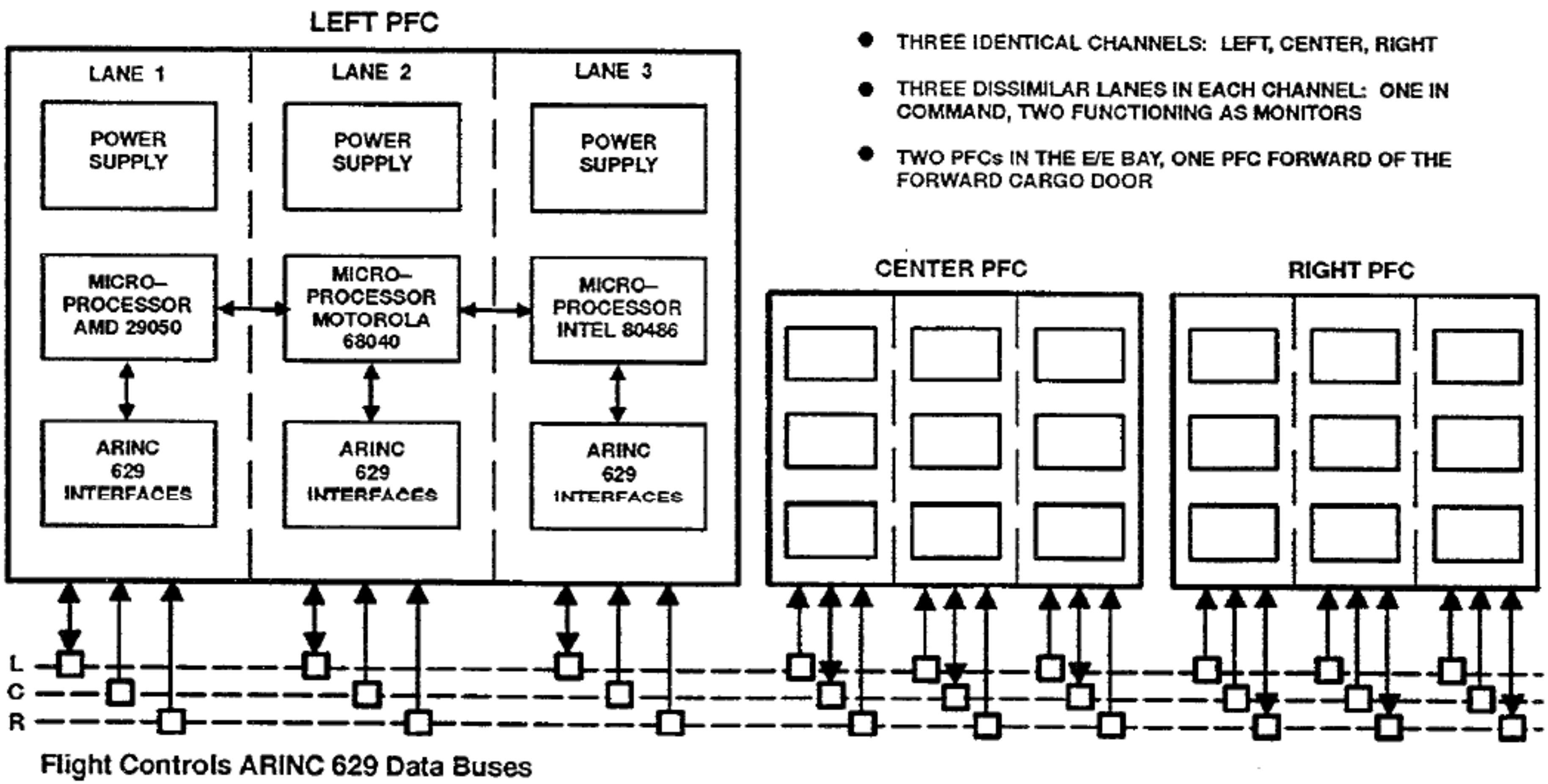

Figure 5 Primary Flight Computer Channel Architecture

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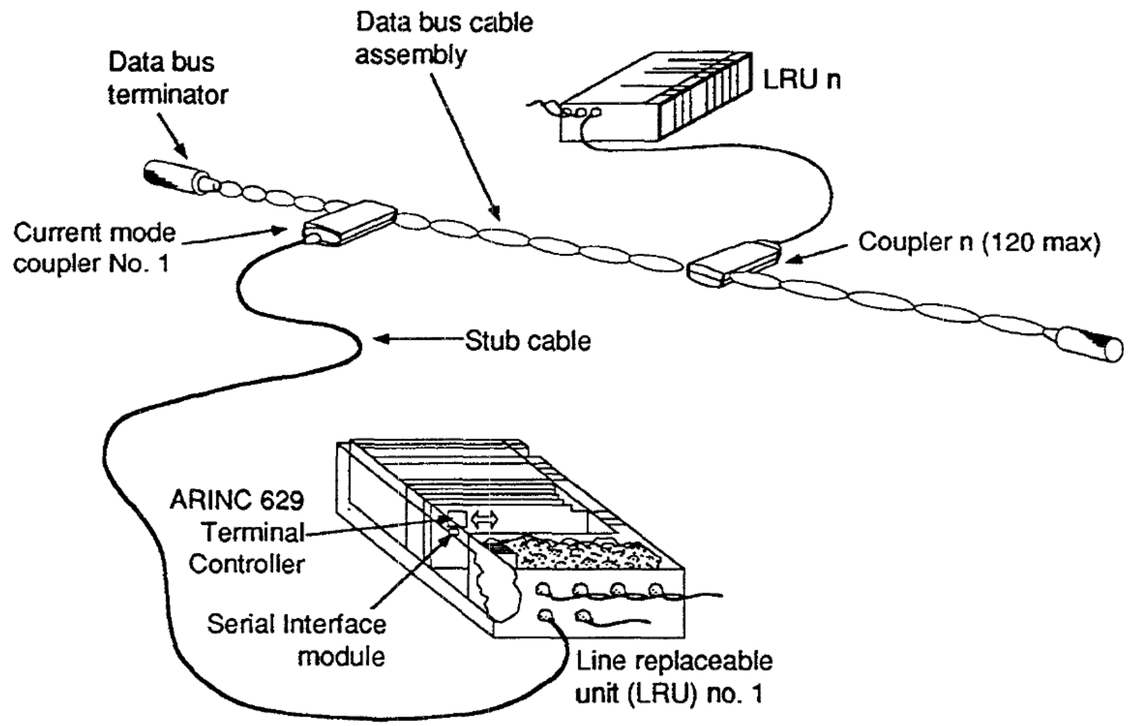
- ARINC 629 Digital Data Bus
  - time division multiplex system, up to 120 users
  - terminal access is autonomous, terminal listens, waits for quite period and transmits

3 protocol timers insure fair access in round robin fashion



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– receiver listens to all traffic and determines which wordstrings are needed

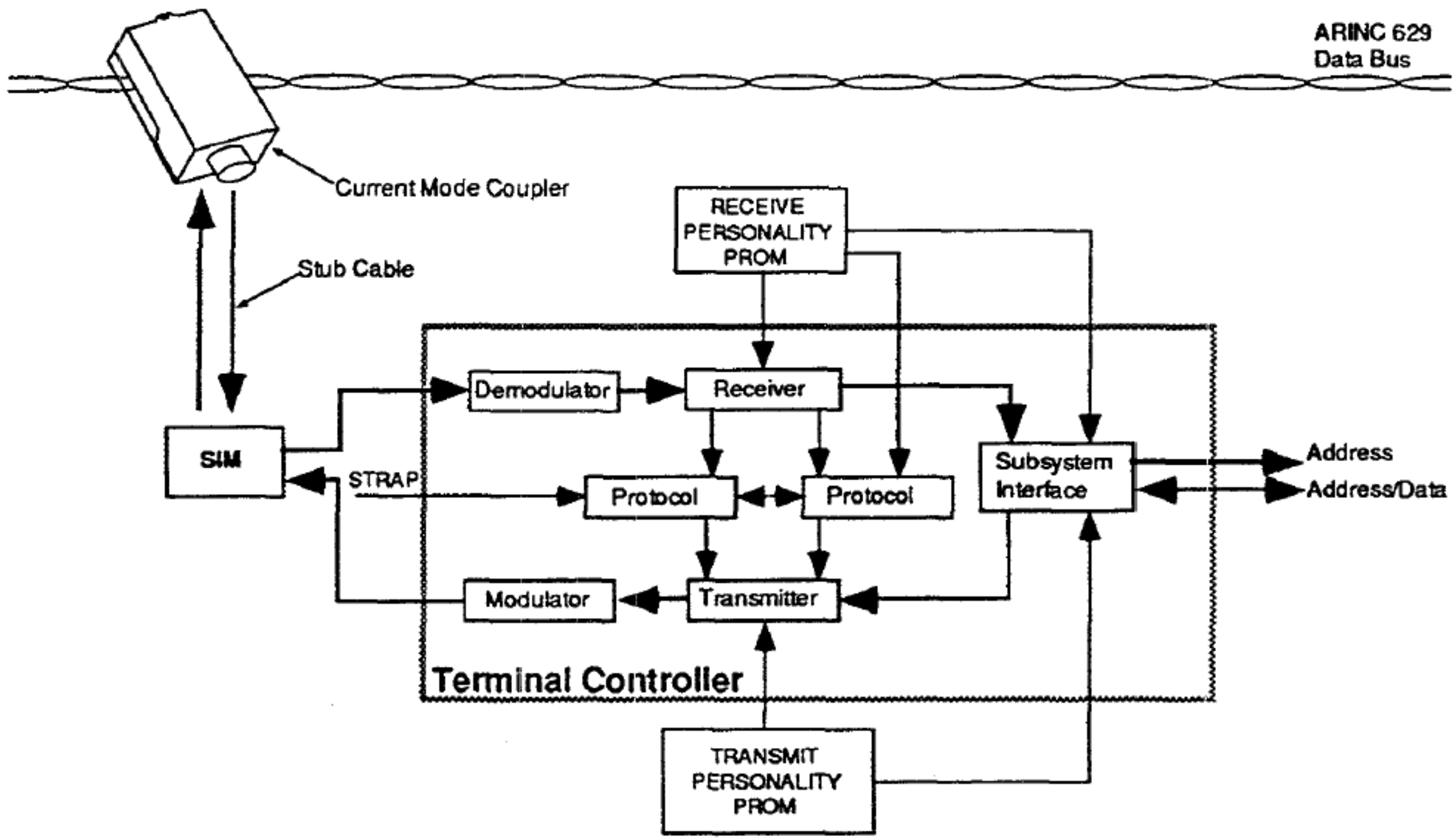

Figure 7 ARINC 629 Functional Block Diagram

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- ARINC 629 bus requirements:
  - data bus availability requirements
  - tolerance to error occurrences of 1 in 10^8 bits
  - tolerance of aperiodic bus operation
  - transmission requirements to provide indication of output data freshness and to not output split-frame data
  - common CRC algorithm

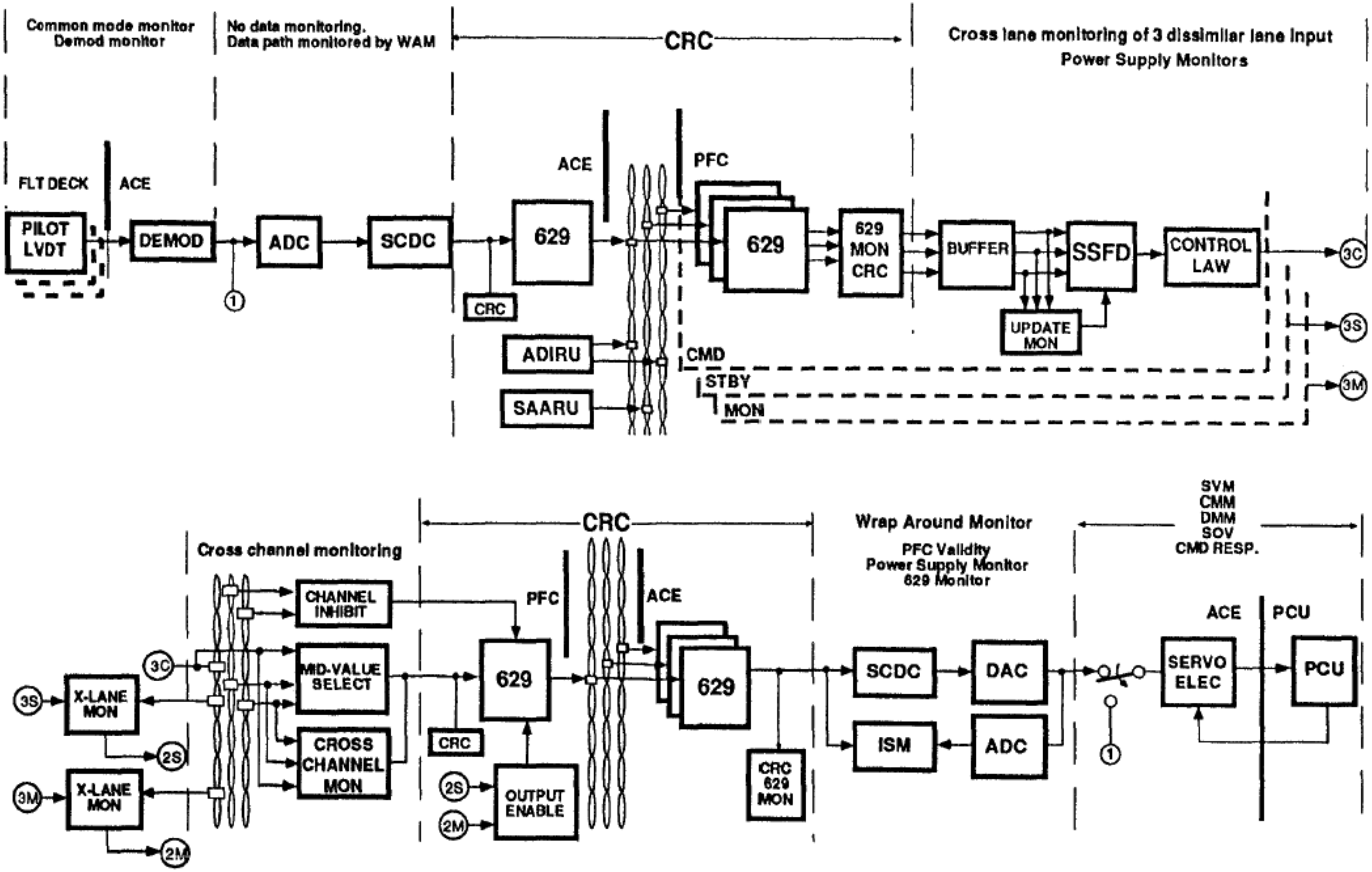

Figure 8 FBW Forward Path Signal Monitor

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- Common Mode & Common Area Fault
  - Component and functional separation. Resistant to
    - maintenance crew error or miss-handling,
    - impact of objects, electric faults, electric power failure, electro-magnetic environment, lightning, hydraulic failure, structural damage
  - Separation of components
    - multiple equipment bays
    - physical separation, (including wiring)
    - separation of electrical and hydraulic line routing

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- Functional Separation
  - Left, Center, Right flight control electrical buses
  - Unit transmits on only 1 ARINC 629,
    - each unit transmits on its dedicated bus, but monitors the others
    - unit failure can effect only single bus
  - Distribution of actuator control,
    - i.e. L/C/R units control actuators using L/C/R respective buses.
- Dissimilarity
  - dissimilar microprocessors
  - dissimilar compilers
  - dissimilar control & monitor functions
  - dissimilar inertial data systems
  - ACE direct mode allowing bypassing of buses

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- Safety Requirements
  - PFC: probability of 10^{-10} /h for
    - functional integrity (active failures affecting plane structure)
    - functional availability (passive failures)
  - 10^{-10} /h for
    - all PFC operational
    - any single lane fault
  - 10^{-10} /h per auto-land operation for:
    - full operational system
    - single lane fault in any/all PFC
    - single PFC fault
    - single PFC fault & multiple single lane faults
  - No single fault should cause error without failure indication
  - No single fault should cause loss of $>$ 1 PFC

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- Redundancy Management
  - PFC inter-lane communication within each PFC channel
  - Frame synchronization
  - (Input) Data synchronous operation
  - Median value selection
  - Cross-Channel Consolidation and Equalization
  - PFC external resource monitoring
  - In addition to ARINC bus: private cross-lane data bus for
    - frame synchronization within a PFC channel
    - data synchronization within a PFC channel
    - cross-lane data transfer

Redundancy Management: typical control path

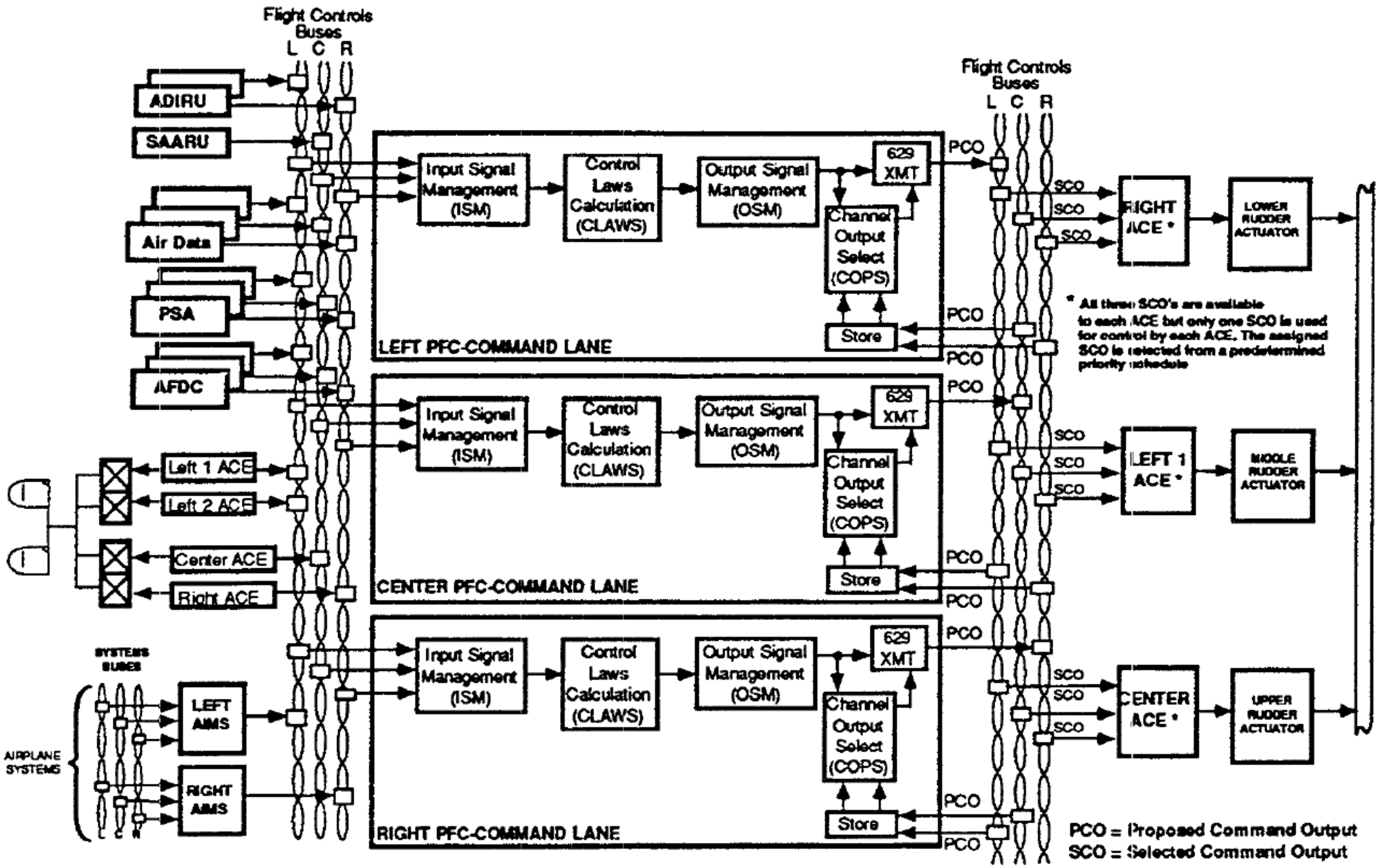

Figure 9 PFC Redundancy Management Overview (Typical Control Path)

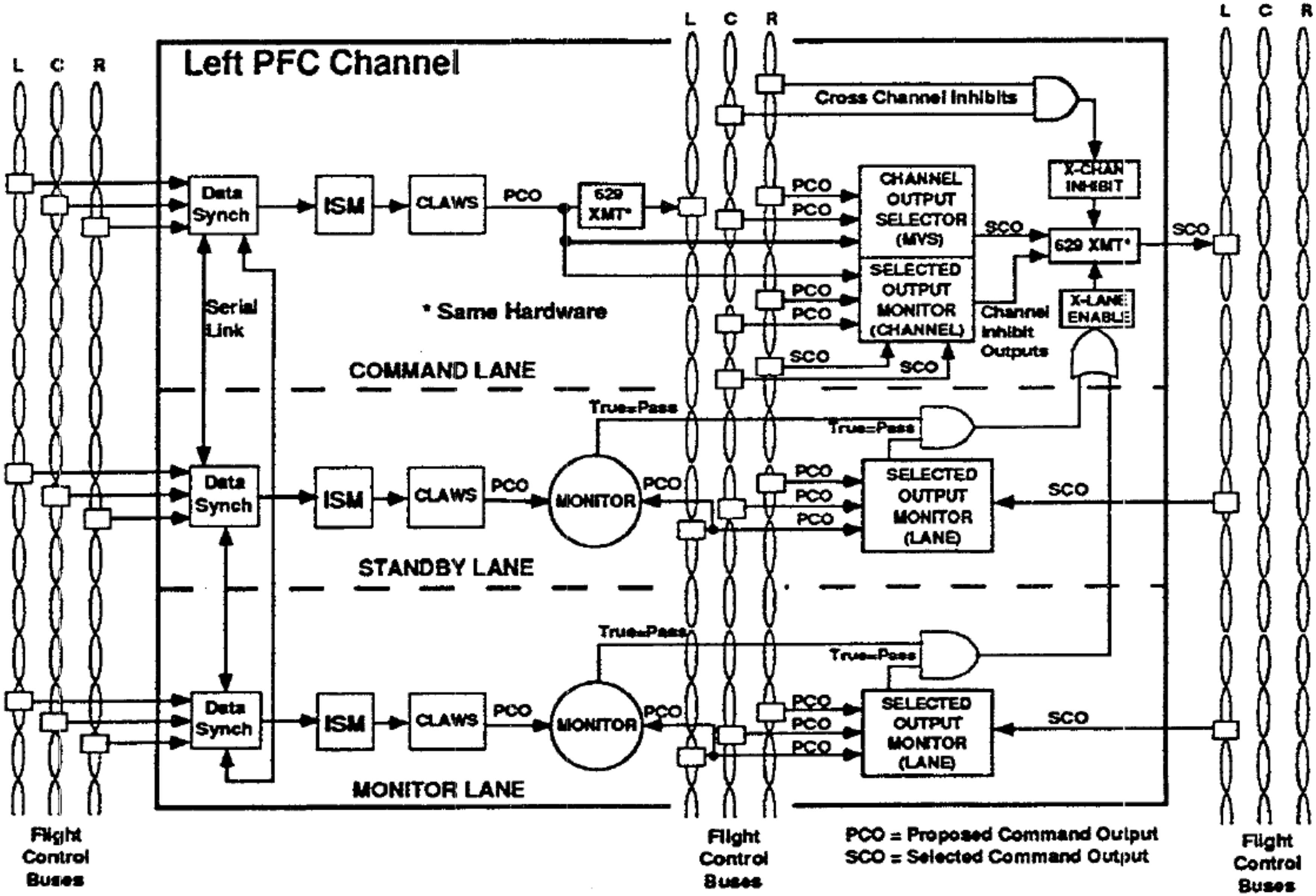

Figure 10 PFC Lane Redundancy Management (Output Signal Monitoring)

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- Synchronization
  - Frame Synchronization
    - to allow tight cross-lane monitoring
    - convergent (mid-point selection) frame synchronization
    - tight synchr. within a few microseconds (what about worse case?)
  - Data Synchronization
    - 2 MHz ARINC 629 => transmit duration > 20us
    - 20us >> frame synchronization time, thus giving sufficient time for data synchronization
    - all PFC lanes are synchronized to the same data set.
      - this data is then used at the beginning of each computation frame
      - allows tighter tracking between lanes
    - occasional PFC lane differences are tolerated

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- Monitoring

  Dual role of PFC lanes

  - Command role:
    - only one lane
    - will send proposed surface command to ARINC 629
    - output is result of median select
    - other ARINC 629 receive command from other PFCs
  - Monitor role:
    - “selected output" monitoring
    - cross-line inhibit hardware logic
  - Cross-Line and Cross-Channel monitoring
  - Critical discretes and variables are equalized between PFC channels